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Design of a Novel Current Mode Charge Pump for Very-Low-Voltage Applications in 130 nm SOI-BCD Technology

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Abstract— A novel charge pump with current mode control suitable to work under a very-low-voltage supply is proposed in this paper. The proposed charge pump consists of two sections. The first section is a power switches stage which consists of seven cascaded DEPMOS power switches. The second section is a low voltage stage which consists of a Low Voltage Level Shifter, Current Mode control, Follower Amplifier, Error Amplifier, Soft Start Comparator, and Skip mode & Over Voltage Comparator. The charge pump has been designed, simulated, and layout in Cadence using TSMC 130 nm SOI technology with LDMOS transistors, which have very low on-resistance. The input range of the charge pump is 2.7–4.4 V, and it can supply up to 100 mA load current. The maximum efficiency is 90%, and the chip area is only 0.597 mm².

Keywords— DC-DC Converter, Energy Harvesting, Switched Capacitors Converters, Low Voltage, CMOS Technology.

I. Introduction

BATTERY-POWERED products such as cellular phones, audio equipment, portable tools, and many other products usually require a voltage converter that transforms the battery voltage output into a stable system supply which is often at a different level. Many applications require a supply voltage of 3.3V or 5V with a 5% tolerance. The traditional art to perform the voltage conversion uses an inductive DC-DC converter [1]-[4], but sub-micron technologies are making charge pumps more and more attractive. The inductive DC-DC converter is characterized by having a high-power efficiency over wide input voltage, low quiescent current, high transformation ratio, large inductor, and low Electromagnetic Interference (EMI) difficult to reach. However, the major advantage of a charge pump [5]-[8] is that it stores energy in a capacitor instead of an inductor. Inductors are voluminous, can saturate, produce EMI, and are quite expensive. Many customers dislike inductive DC-DC converters for this reason. Charge pumps have the image of being noisy, having high output voltage ripple, and being inefficient, but new design- and process techniques do away with these problems.

Due to their topology charge pumps need twice the number of switches than inductive converters. Asynchronous boost converter needs two switches, a charge pump voltage doubler needs at minimum four switches [9],[10]. Having a specific chip area available for switching transistors, the current path in a charge pump is four times more resistive than that in the inductive converter. The last wafer fabrication processes with their short MOS-channel lengths, thin gate oxides, narrow transistor pitches and the capability to control the parameters more precisely deliver MOS-transistors with extremely high current drive capability in a given chip area, such that overall, charge pumps can easily compete with inductive converters. These switching transistors with their high I-Drive make it possible to produce integrated charge pumps with output currents beyond 200 mA. The entire structure of this paper is given as follows: The operation and topology of the regulated voltage doubler are described in section 2. The description and functionality of the proposed charge pump voltage converter in section 3. The simulation results and layout in section 4. Finally, the conclusion in section 5.

II. Regulated Voltage Doubler Topology & Operation

Many methods and techniques to regulate the switch capacitor of the charge pump voltage converter. The simplest method is to follow the switched capacitor doubler with a low drop out (LDO) regulator [11], which provides a controlled output while reducing the ripple of the switched capacitor converter. However, this technique brings some difficulty to the circuit and decreases the usable output voltage by the LDO regulator's dropout voltage. Another solution to regulation is to adjust the duty cycle of the switch control signal with the output of an error amplifier [12], which compares the output voltage to a reference. This method is close to those used in inductor-based switching regulators; however, it often

necessitates the implementation of a pulse width modulator (PWM) with suitable control circuitry. Nevertheless, this method is extremely non-linear and necessitates a long time constant. The easiest and most efficient approach for achieving regulation in a switched capacitor voltage converter suggested in this paper is to use an error amplifier to regulate not only the ON resistance of one of the switches but also the current of one of the switches to supplement Ron control with current source control, which increases system stability.

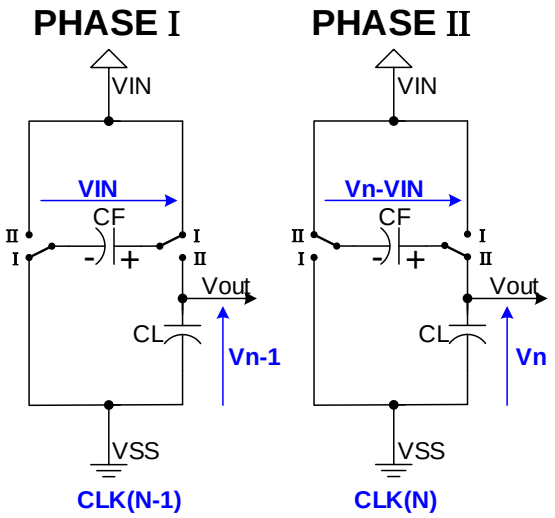


Fig. 1 Block diagram of the operation of the charge pump voltage doubler

Figure 1 shows an inductor-less voltage doubler. The node V_{OUT} is made up of four switches, a "flying" capacitor C_F, and an output capacitor C_{OUT}. A Charge Pump operating period can be divided into three phases: Phase I: The switches and capacitors are ideal, and the voltage doubler begins in PHASE I; in this situation, the capacitor C_F is initially charged to Vin, and C_L is thought to have no initial charge. Phase I to phase II: According to the law of charge conservation, when two capacitors are connected, the cumulative charge on the pair equals the sum of the initial charges on the capacitors $C_{F-} = V_{in}$ & $C_{F+} = 2*V_{in}$. C_F is Connected to C_L. The Charge Stored in C_F is Shared with C_L V_{OUT} is Fixed by V_{in} plus a voltage due to the Charge Redistribution. The expression of the V_N can be extracted from the (1):

$$C_F*V_{in}+C_L*V_{N-1}=C_L*(V_N-V_{in})+C_L*V_{in} \quad (1)$$

$$V_N=a*V_{N-1}+b*V_{in} \quad (2)$$

Where $a=\frac{C_L}{C_L+C_F}$; $b=\frac{2*C_F}{C_L+C_F}$

By assuming the initial value of $V_{OUT} = 0$; After N period the V_N will be (3)

$$V_N=\frac{1-a^{N+1}}{1-a}*b*V_{in}=2*\left(1-a^{N+1}\right)*V_{in} \quad (3)$$

When N→∞ Since $a<1$: $V_N = 2*V_{in}$

The switches periodically toggle between phase I and phase II so energy is transferred from the battery V_{in} to the Load V_{OUT}. With no-load current the max. output voltage V_{OUT} is two times the input voltage V_{in} for a voltage doubler. A single-ended charge pump [13] delivers energy to the output only during the "transfer phase (B)". When the charge pump is in the "charge phase (A)" the output capacitor C_{OUT} has to deliver the load current. Since C_{OUT} is periodically charged and discharged to a certain degree the output voltage has a ripple. This ripple can be avoided using a push-pull charge pump [14]. It consists of two single-ended charge pumps, as described above which work in anti-phase. When one single-ended charge pump is in the "charge" phase the other one is in the "transfer" phase such that there is a continuous delivery of energy to the output. Since the output capacitor C_{OUT} is not charged and discharged anymore the push-pull charge pump produces an extremely low output voltage ripple (theoretically zero). C_{OUT} eliminates possible switching spikes as shown in Fig. 2.

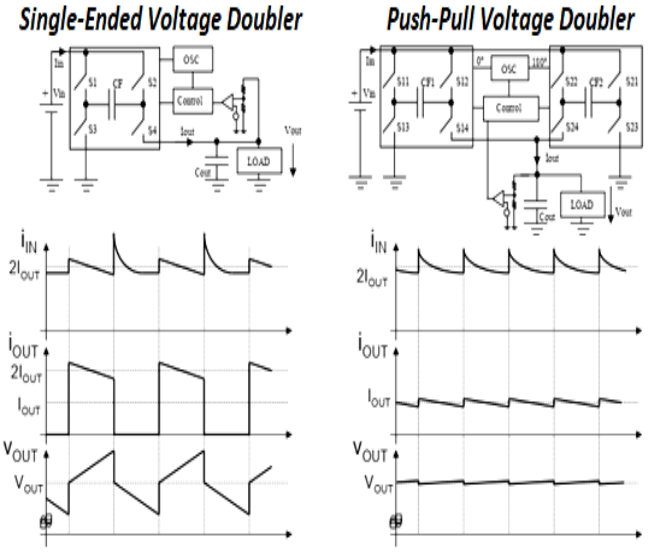


Fig. 2 Charge Pump Converter - Principle of Operation

III. Description & Functionality of the Proposed Charge Pump Voltage Converter

The block diagram of the proposed charge pump is shown in Fig. 3, which consists of two sections, the power MOS and high voltage section, and the low voltage section.

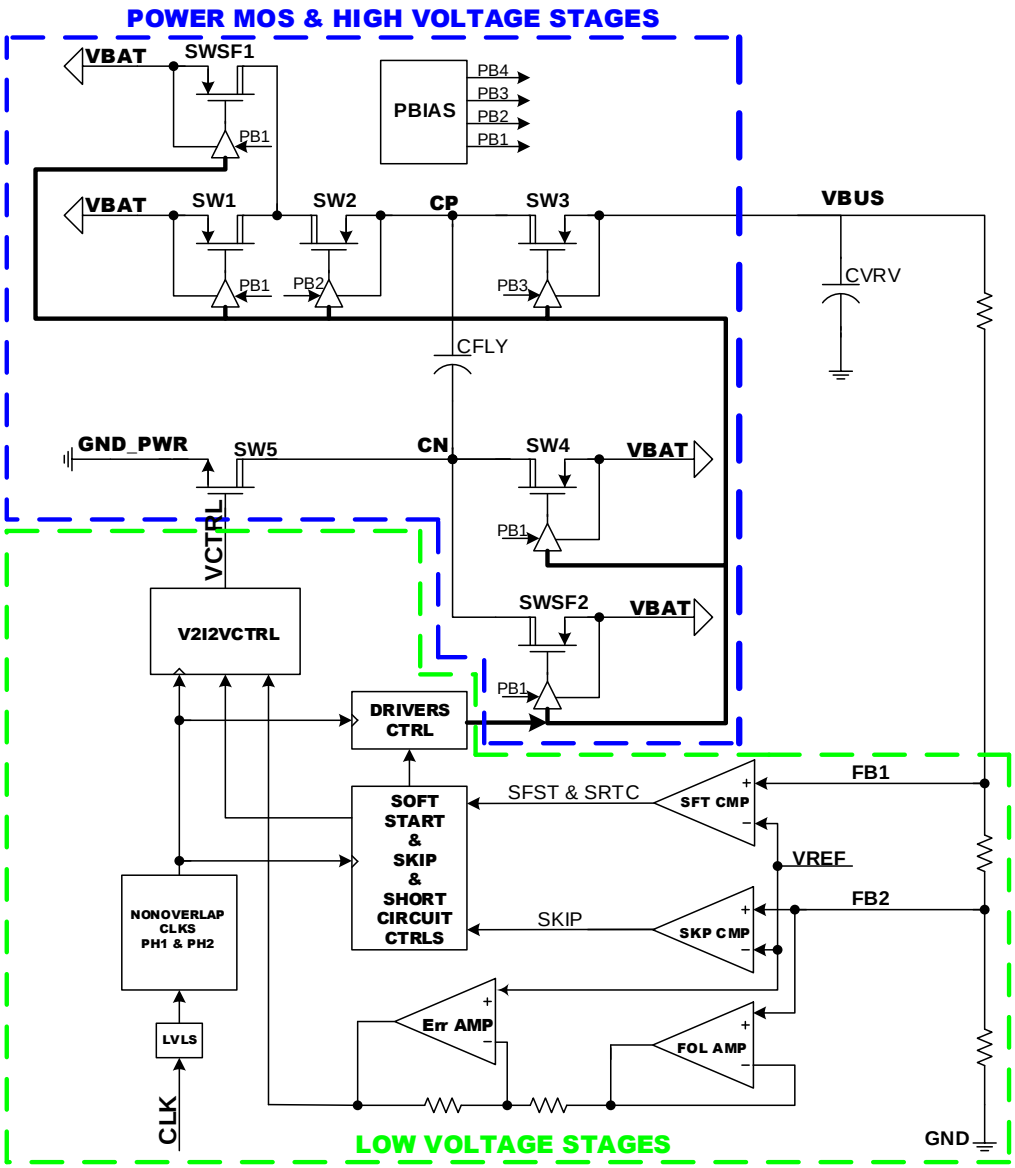


Fig. 3 The proposed charge pump block diagram

The first section contains five power switches plus two power soft start switches, the type of switches is DEPMOS switches. The second section of the proposed circuit design contains a low voltage level shifter, a follower amplifier, error amplifier, current-mode control, soft start comparator, and skip mode and over-voltage comparator.

A. Power Switches & Power Soft Start Switches

Seven switches are used in the proposed circuit as mentioned five power switches (SW1, SW2, SW3, SW4, SW5), and two power soft start switches (SWSF1, SWSF2), which the size of these switches is increased to support low battery voltage of 3.0 V. Fig. 4. illustrated the variation of the switch ON resistance Ron in weak process with sweeping temperature between -40° to 140°as the simulation graph shows a Ron of 467mΩ, as well it shows good linearity of Ron with temperature variation. Fig. 5. represents the variation of the voltage of the five power switches (SW1, SW2, SW3, SW4, SW5) by applying on VBUS 7V. The simulation graph represents the voltage behavior of the five power switches by variating the voltage VBUS from 0 to 7V.

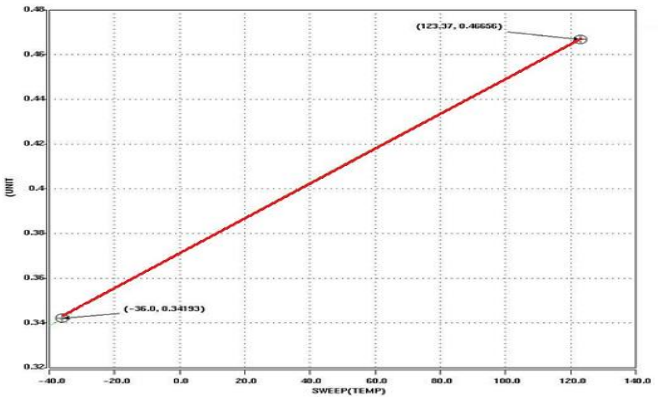


Fig. 4 Simulation results of the variation of the Ron with temperature variation

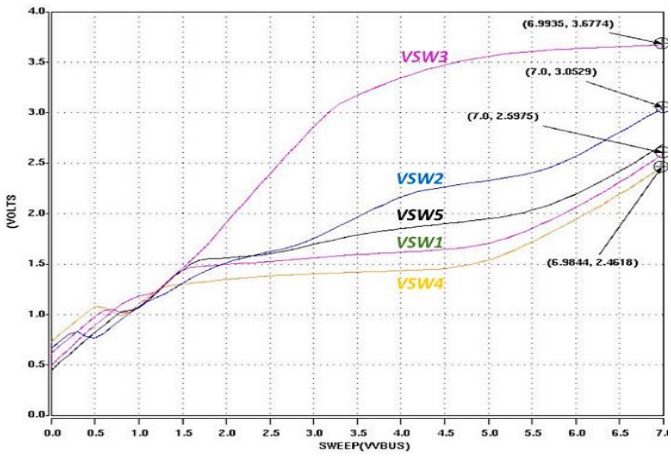


Fig. 5 Simulation results of the variation of the (SW1, SW2, SW3, SW4, SW5) voltages with VBUS variating from 0 to 7V

B. Drivers

The drivers allow the control of the power switches, behave as an intermediary between the switches and the drivers control unit. For each switch used in this paper a driver is connected to their gates, the driver circuit architecture is based on a high voltage level shifter. The drivers used in this paper were designed to be independent of the non-overlap clock generator [15].

C. Low Voltage Level Shifter

The low voltage level shifter used in this architecture to command the non-Over-Lop clocks that will generate PH1 and PH2 by level shifting the clock signal, the circuit design of the level shifter is presented in Fig. 6.

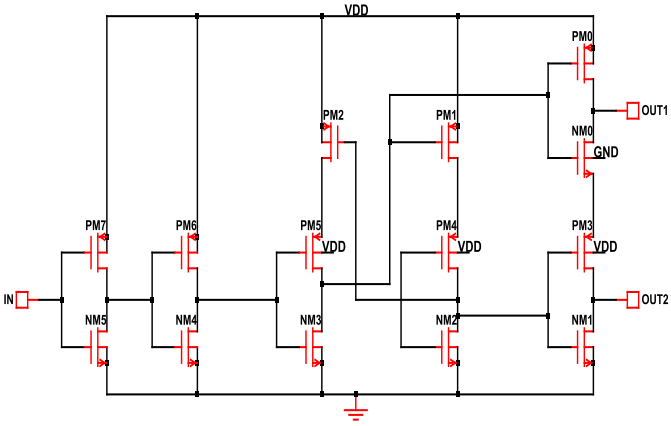


Fig. 6 Circuit design of the Low Voltage Level Shifter

D. Error Amplifier & Follower Amplifier

The error amplifier is used to amplifies the voltage signal based on the difference between voltage reference and the voltage generated between R4 and R5. The main use of the follower amplifier in the proposed architecture is to provide a low impedance output to provide high current output and or high bandwidth for a high capacitance load. The circuit design used for each amplifier is represented in Fig. 7 [16]. The circuit design of the operational amplifier consists of the differential input stage, common-source stage, and output buffer. The gain of each stage of the operational amplifier are expressed by the following (4), (5), and (6):

$$A_{V1} = g_{m1} * \left(r_{ds2} \square r_{ds4}\right) \tag{4}$$

with $g_{m1} = \sqrt{2\mu C_{ox}\left(\frac{W}{L}\right) I_{D1}}$ and $I_{D1} = \frac{I_{Bias}}{2}$

$$A_{V2} = -g_{m7} * \left(r_{ds5} \square r_{ds7}\right) \tag{5}$$

$$A_{V3} \cong \frac{g_{m8}}{g_{m8} + C_L + g_{mb8} + g_{o8}} \tag{6}$$

The input of the closed loop is step to Vref=0.75V, with VBUS of 4.85V we can express output voltage by the following (7):

$$V_{out} = (1+B) * V_{ref} - (A * B * V_{Bus}) \tag{7}$$

With A has a value of 0.15, and B variation from 10 to 40, which are depending on the input of the amplifier. The AC and DC simulations for the amplifier used in the proposed design are shown in Fig. 8. (a) and Fig. 8. (b), the simulation result in a weak and a strong process with a phase margin of 55 deg. The results of the AC and DC simulation show a good response and stability of the follower amplifier.

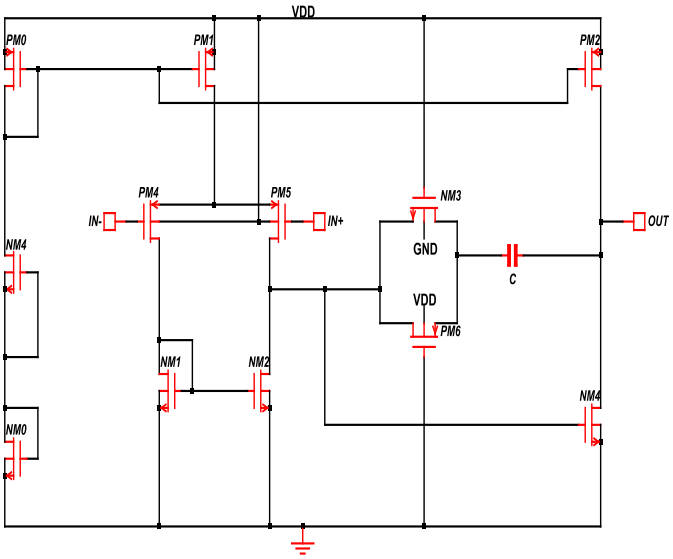
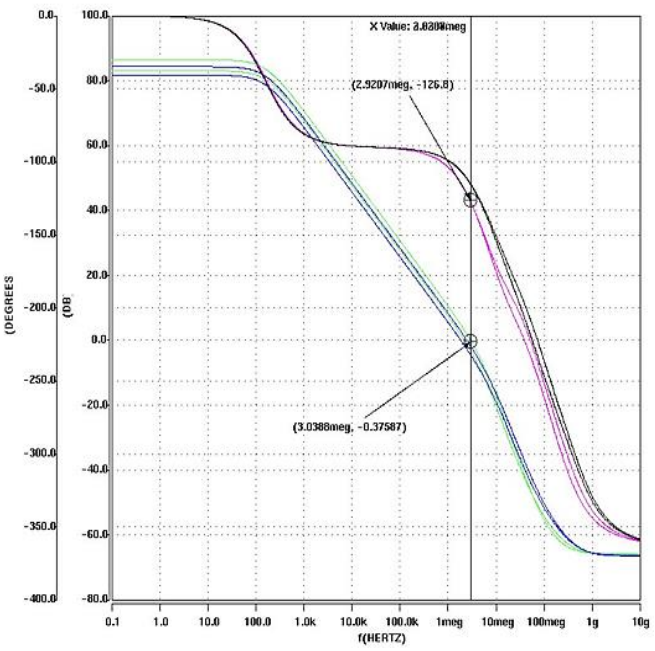
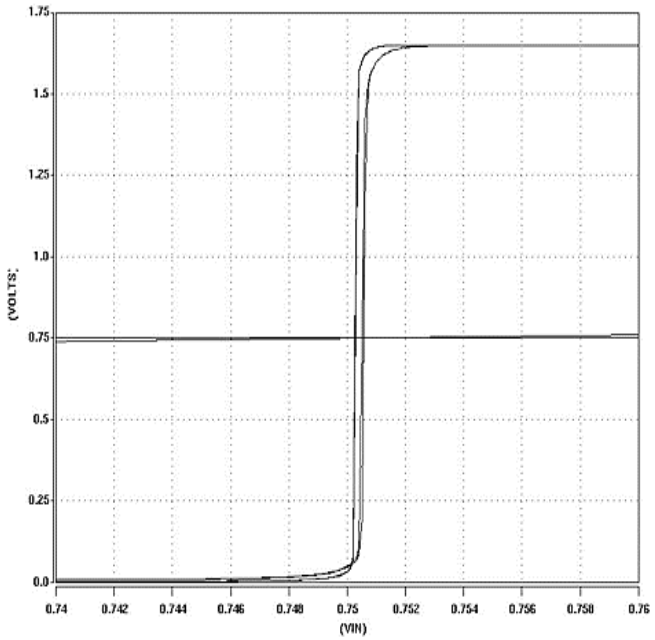


Fig. 7. Circuit design of the amplifier used as error amplifier and follower amplifier



(a)



(b)

Fig 8. Simulation results in (a) AC analysis and (b) DC analysis

E. Soft Start Mode Comparator

The soft-start comparator is employed to compare the voltage coming from the feedback resistors FB1 with a voltage reference in order to generate a voltage to be used in the next block, the circuit design of the Soft Start comparator is shown in Fig. 9. The soft-start mode allows to force the battery voltage VBAT in case of no-load and VBAT-IRdrop in case of load that limit the inrush at the startup.

F. Skip Mode & Over Voltage Mode Comparator

The output voltage Vout is compared to a reference standard in skip mode. If Vout is too low, the charge pump is engaged and energy is delivered to the output. The charge pump is switched off until the voltage on the output level exceeds the reference level. The amount of energy delivered is determined not only by the switch resistance but also by the supply voltage and the frequency of the charge pump. The skip mode and over-voltage comparator circuit design are the same as the soft-start comparator circuit architecture as represented in Fig. 9, this comparator is used to compare the voltage generated by the second part of the feedback resistors FB2 with the same voltage reference VREF. As well the voltage emitted from the skip mode and over voltage comparator will be employed in the Soft Start & Skip & Short circuit control.

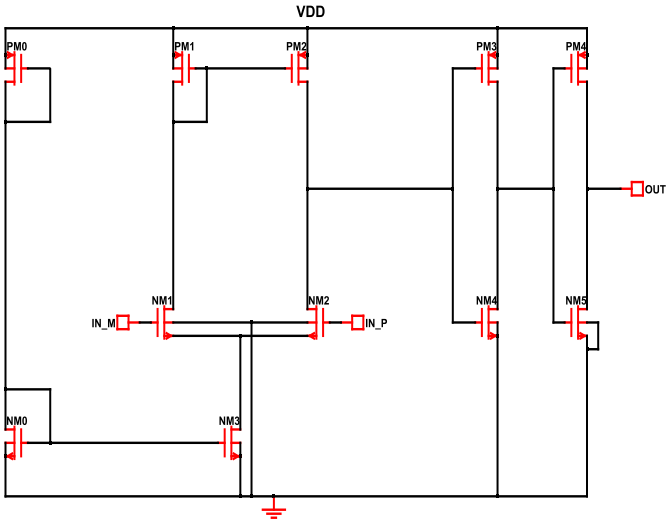


Fig. 9 Circuit design of the comparator used in soft start mode and skip mode

G. Current Mode Control Circuit

The current mode control is employed to command the driver control by generating VCTRL. The current mode control circuit design is shown in Fig. 10. The current mode control architecture consists of five levels. The voltage to the current level, the current comparator, and current clamp, the current to voltage, the follower, and the new current-mode feedback allow better functionality at low battery voltage. The current mode control was changed in order to have a current limitation which functioning of IREF and VBUS VCN, with a supply voltage of 1.8V. The simulations graphs are for the substrate switching noise of the current mode control, Fig. 11 represent the variation of the current ICTRL and IVSS in transient mode, with ICTRL Is the current flowing in the I2V stage is 49.3mA, and IVSS is the current going to the substrate is 26,9mA with having a 5 Ohms series Resistor.

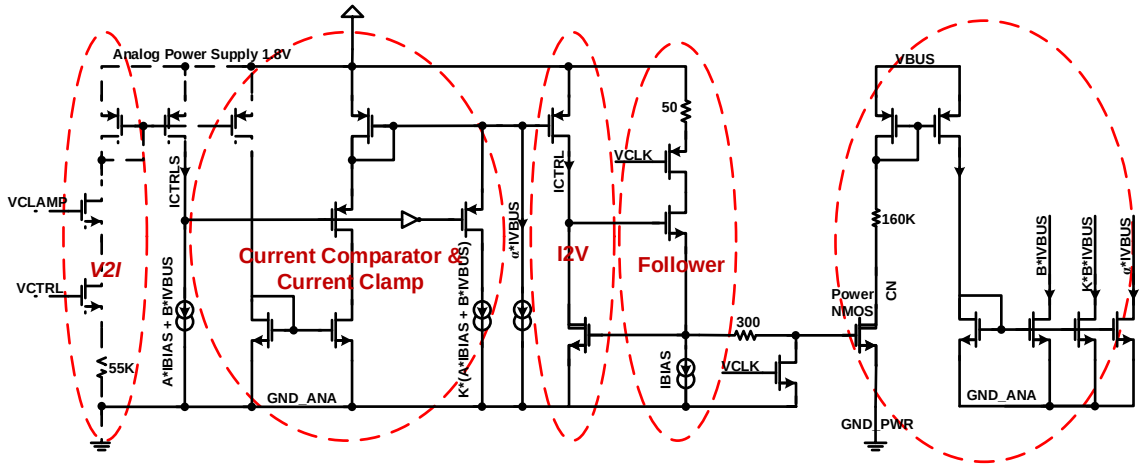


Fig. 10 Current mode control architecture

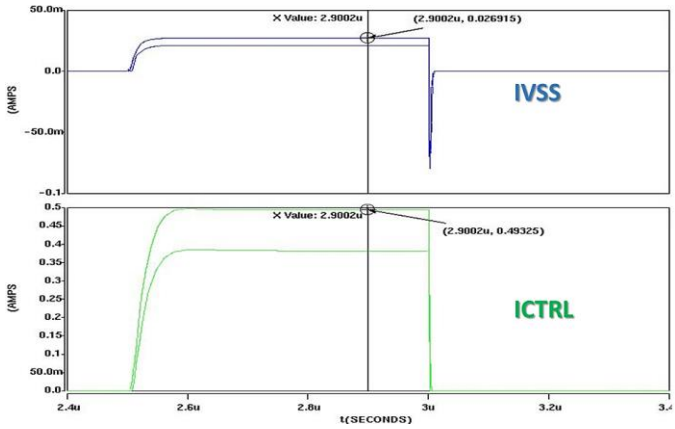


Fig. 11. Simulation results of the current IVSS & ICTRL in transient mode

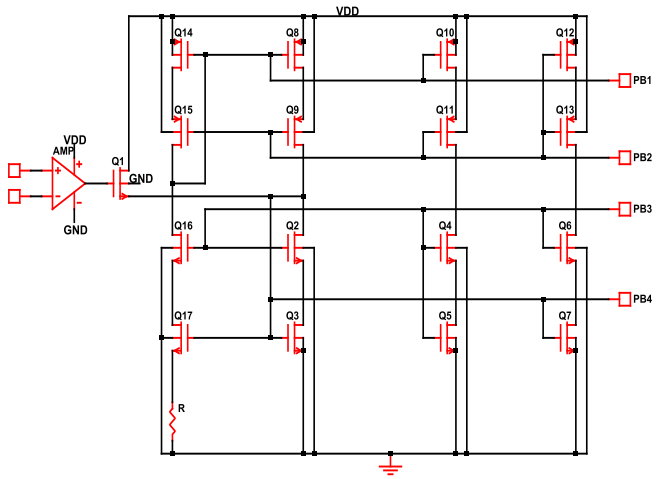


Fig. 12 PMOS Bias Voltage architecture

H. *Non-Overlap Clock Generator Circuit*

Generally, the clock signals must be non-overlapping to guarantee that charge is not lost. The non-overlap clock generator is employed to command the current mode control, the drivers control, and the soft start and skip and short circuit control by generating two clock signals PH1 and PH2. The function of the non-overlap clock circuit is that the non-overlap clock signals running at the same frequency, and there is a time between the pulses that none of them is high.

I. *PMOS Bias Voltage Generator Circuit*

The PMOS Bias voltage is employed to command the drivers that are connected to the switches by generating four signals PB1, PB2, PB3, and PB4. The PMOS Bias voltage circuit design is represented in Fig. 12.

J. *Drivers Control Circuit*

The drivers control is a digital block used to check and command the drivers, the driver control circuit design is based on logic gates (inverters, OR, AND) as shown in Fig. 13, all components are supplied by a value of 1.8V.

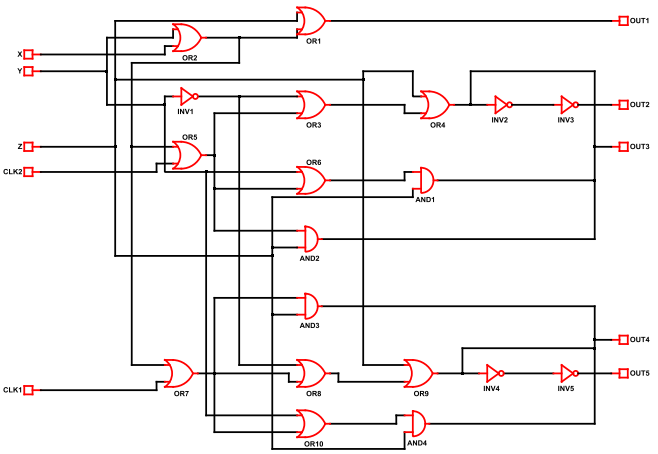


Fig. 13 Driver Control circuit design

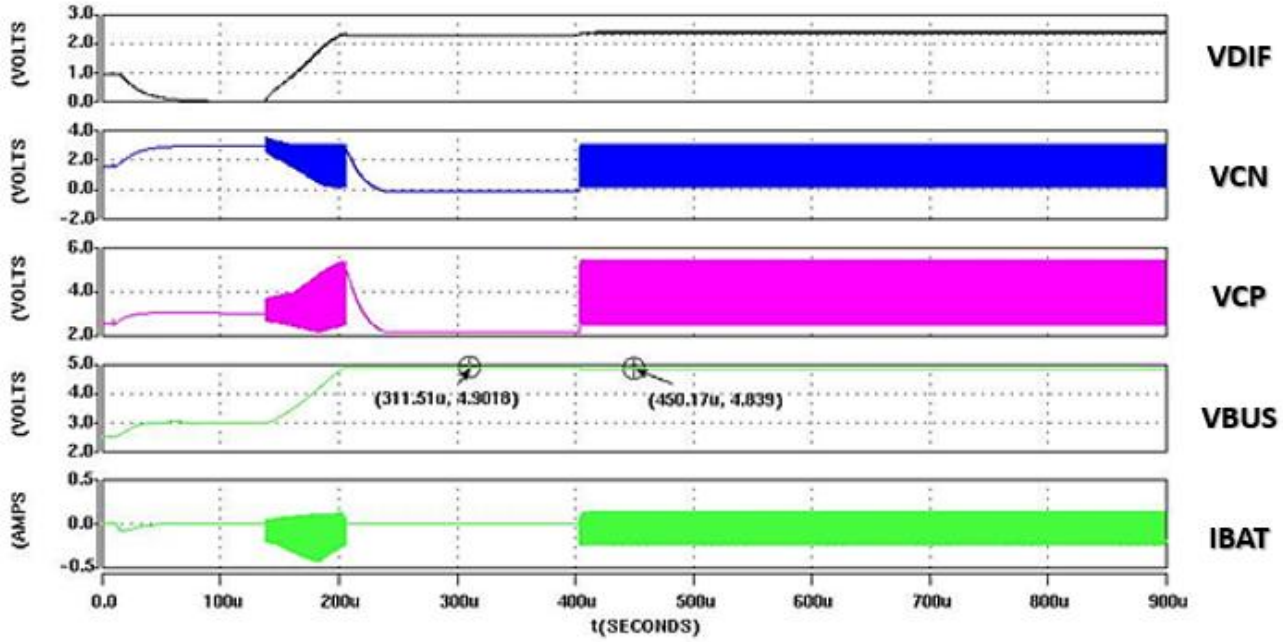
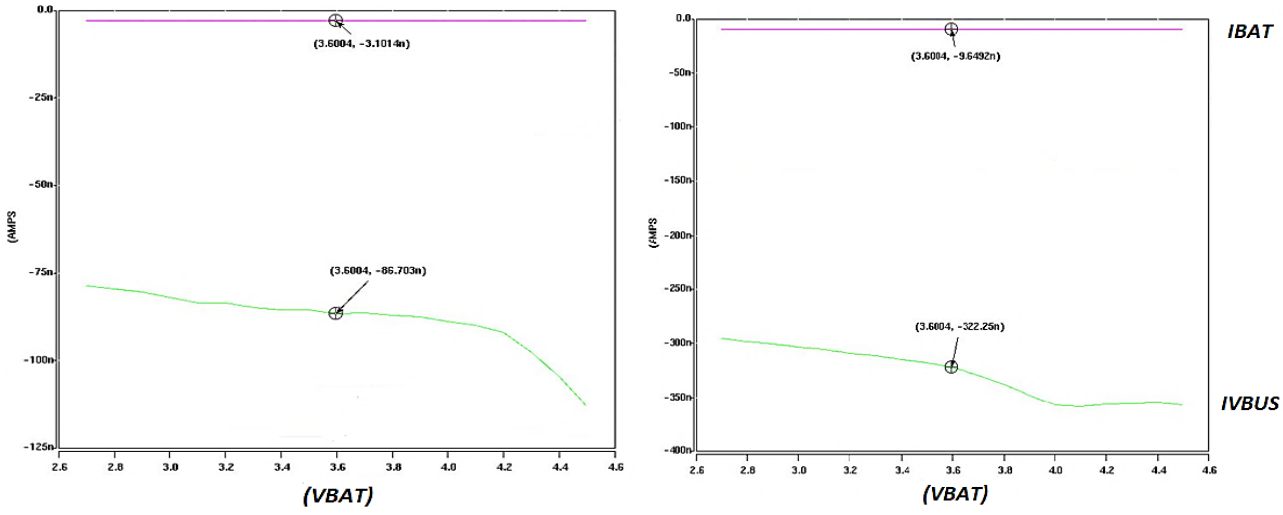


Fig. 14 Simulation results of the functionality of the proposed charge pump



(a) (b)

Fig. 15. Simulation results of nominal voltage leakage for IBAT and IVBUS in: (a) Nominal Process, and (b) Strong Process

IV. Simulation Results

The proposed architecture design is simulated in Cadence using TSMC 130 nm SOI technology with LDMOS transistors, which have very low on-resistance. The functional simulation of the proposed charge pump is shown in Fig. 14, by simulating the voltage differential that is used in the test bench (VDIF), the voltage in nods CP and CN in power MOS and high voltage section (VCP, VCN), the voltage of CVRV capacitor (VBUS), and battery current (IBAT). The simulation shows that the proposed architecture has good reading and response, with a battery voltage of 3V, and temperature of 30°C with a parasitic resistor on the power devices.

Fig. 15. display nominal voltage leakage for battery current (IBAT) and current (IVBUS) by variating battery voltage from 2.7V to 4.5V in the nominal process (a), and strong process (b). for the nominal process at 3.6 V for battery voltage, IBAT is 87nA, and IVBUS is 37nA. and for the strong process at the same battery voltage value of 3.6V IBAT is 333nA, and IVBUS is 127nA. Fig. 16. display the stability of the proposed charge pump generating a phase margin of 78 Deg. This simulation is essential to calculate how close the system's second pole is to triggering instability. The phase change cannot be greater than 180°. Generally, any degree greater than 45° is permissible. The greater the phase margin, the greater the system's stability.

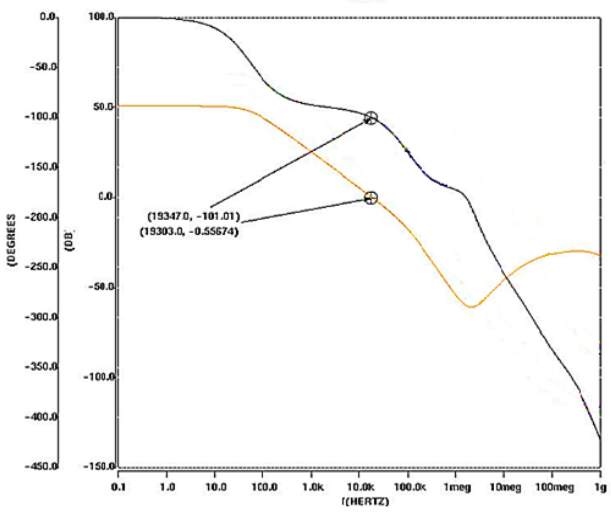


Fig. 16 Stability simulation result

Fig. 17. shows the efficiency of the system as a function of the output power with a frequency of 1 MHz, the peak efficiency of the system is 90%. Fig. 18 display the layout of the proposed circuit design of the current mode charge pump. The switches occupy the majority of the chip's area, also the layout respects the design rules and the design constraint information. The major aspect of these rules is to achieve a high overall yield and durability by using the smallest practicable silicon area. These rules typically prescribe the minimum permissible line widths such as metal and polysilicon interconnects, as well as the minimum allowable feature dimensions and separations between two such features, among other things. The surface area of the proposed architecture is 0.597 mm². Finally, Table 1 displays a summary and comparison performance of the proposed charge pump and other works.

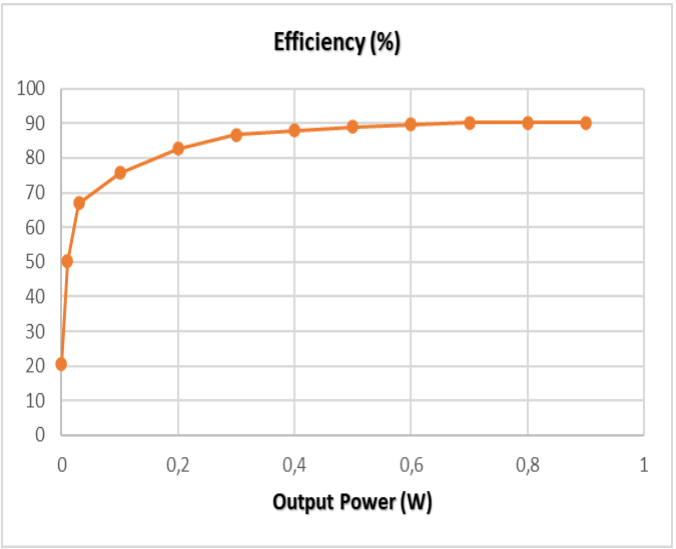


Fig. 17 System efficiency versus output power with fin=1MHz

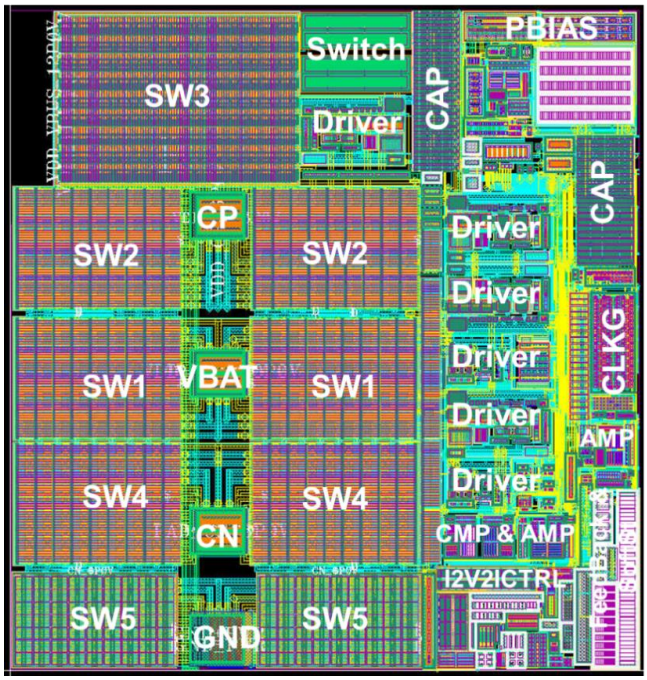


Fig. 18 Layout of the proposed charge pump

Table 1. Summary and Comparison Performance

	[17]	[18]	[19]	This Work
CMOS Process	180nm	65nm	250nm	130nm SOI
Topology	4-Stages Charge Pump	4 Stages Charge Pump	3 Stages Charge Pump	Voltage Doubler Charge Pump
Load current	10µA-1mA	n/a	3.33mA	100mA
Efficiency (%)	84.7	66	84	90
Chip Area (mm²)	0.6	0.17	0.5	0.597

V. Conclusion

In conclusion, a novel current-mode charge pump for very low voltage applications has been successfully designed in 130nm SOI-BCD technology. Circuit design, simulation, analysis, and layout design are all included in this study. The performance of the current mode charge pump is enhanced in this study. The proposed charge pump includes a power switch stage made up of five cascaded DEPMOS power switches, as well as a low voltage stage composed of a low voltage level shifter, current mode control, follower amplifier, error amplifier, soft-start comparator, and skip mode & over-voltage comparator. An efficiency of 90% can be achieved with having an input range of 2.7V to 4.4V, as well as supplying up to 100mA load current, and the total area of the proposed charge pump is 0.597mm². The results show good efficiency and low distortion. The chip possesses super characteristics suitable for

battery-powered devices.

ACKNOWLEDGMENT

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