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A 14-bit High Speed 125MS/s Low Power SAR ADC using Dual Split Capacitor DAC Architecture in 90nm CMOS Technology

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Abstract- The proposed work presents a High speed 14-bit 125MS/s successive-approximation-register asynchronous analog-to-digital-converter (SAR-ADC). A novel-based Dual-Split-Array-Three-Section (DSATS) capacitor DAC (DSATS-CDAC) is employed to increase the linearity and energy efficiency of the digital-to-analog converter (DAC), additional advantage of this work is that, the area is reduced by 59.76% of conventional design. The proposed switching technique of the (DSATS-CDAC) consumes less switching energy. Additionally, bootstrap switching is employed to ensure improved linearity and reduced power consumption.in order to enhance the speed of operation and increase the precision a preamplifier latch based comparator is implemented with the delay of 250ps. The proposed SAR-ADC prototype is implemented in a 90nm CMOS process and consumes a power of 42.8mW at 1V operating supply. The proposed design achieves a figure of merit (FOM) of 37.43 fJ/conversion-step, signal-to-noise-ratio (SNR) of 81 dB, and an effective-number-of-bits (ENOB) of 13.16 bits with a sampling rate of 125MS/s.

Key Words – Successive Approximation Register, Digital to Analog Converter, Dual Split Capacitor DAC, Clock Gated Control Logic, Track and Hold circuit, comparator.

I. INTRODUCTION

In the digital world, electronic devices are widely utilized in different fields of science like communication, transportation, etc. In reality, signals being analog in nature need a ADC to make the digital equipment process the analog signals. The fundamental components in these equipment for the inter conversions are ADC and DAC. Recent advancement in applications emphasis on ADC's having high speed, low power and moderate resolution. Earlier flash ADC's were utilized in such applications. But due to the increased number of comparators needed and exponential increase in power consumption with the resolution of the ADC [1][2], flash ADC's became incompetent for such applications. These drawbacks led to studies sorting out that SAR ADCs are highly efficient compared to other ADCs. Within the world of advancing digital technology, performance analyses of digital CMOS circuits are seeing immense improvements. Improvement in the number of features like smaller area, high speed, etc. has led to scaling down of digital circuits. On the other side, the utilization of longer channel length transistor is used even now, in order to achieve improved circuit performance.

Basic signal processing functions like amplification and filtering are often done in a well-oriented format and price effectively [3] using real time analog circuits. Increasing complexity with the advances in electronic systems, implementation in real time analog signals becomes in-efficient, impracticable and costlier. So as to permit these electronic systems to interface with real time analog signals, the interconversions of analog and digital signals are essential. This concludes that the key matter of fact for the success of those Electronic systems has always been the advances seen in analog-to-digital converters.

II. LITERATURE REVIEW

Globally great efforts are made to develop VLSI systems like ADC's and DAC's that have been one of the most volatile and dominant ones even today in terms of high resolution, power efficiency. This section provides an insight into the research works developed in the last few years to achieve better converter design. Q. Fan and J. Chen, [4] Built a digital-slope 13-bit SAR-Assisted-Time-Interleaved ADC. Here a course and fine ADC's are cascaded to get high resolution and using charge sharing methods to eliminate large power consumption on a chip, the design achieves an SNDR of 63.74dB and FOM of 3.83fJ/conv. K. Kuo, [5] Implemented a Binary Search 10-bit and two SAR ADC's with a two-bit upgrade to Error Tolerance Capabilities. Polineni, S., Bhat, M.S. & Rajan [6], proposed a 10-bit Enhanced MSB Capacitor-Split Switching Technique is used in the fully differential switching scheme for Ultra-Low-Power Enhanced. The proposed design is energy-

efficient and high precision. The switching scheme is energy efficient at 96.88% and capacitor area-efficient at 50% compared to the conventional scheme. The switching scheme features make it ideal for low-power and high-resolution ADC realization. Mao, W., Li, Y., Heng, C.H. and Lian, Y [7]. They describe a multi-segmentation-digital to analogue converter architecture that uses a hybrid switching technique to minimize the overall number of unit capacitors for biological signal processing, SAR ADC is widely used. The NFBWA DAC and hybrid switching method will reduce the DAC part's total unit capacitor count by 87.4%. The results measured show that the ADC achieves 10.47 ENOB and absorbs 110-nW power. Maddox, M. C. W. Coln, Y. Lu, and L. D. Fernando, [8] addresses a high precision converter, it solves the sharing of passive charges by SAR ADC. A passive charge sharing design with one reference cap per bit and a short switch is proposed for SAR ADC, as well as a calibration method that solves the steps needed to attain 16-bit linearity. M. Kulkarni, C. Parikh, and S. Sen, [9] demonstrated a Systematic Approach for Determining Capacitors' Weights in Non-Binary Redundant SAR ADCs' DAC. The analysis brings out that the non-binary redundant SAR ADC provides SNR enhancement along with the speed boost. The proposed algorithm addresses the weights of the capacitors used in the DAC. That weight may be used in both synchronous and asynchronous SAR logic irrespective of the DAC switching scheme. S. Kim and K. Kwon, [10] Presented a hybrid ADC combining capacitive multi-bit / cycle DAC-based SAR ADC with Flash ADC. The design achieves a speed boost and the CDAC capacity size is 2pF which is a significant reduction from a conventional CDAC. Hybridization reduces the data conversion time from 390ns to 140ns.W. Kim et al. [11]. A Low Noise Asynchronous SAR-Assisted Time-Interleaved SAR (SATI-SAR) ADC was implemented. The SWC operation reduces the sizes of the logic blocks in the SAR control loops, along with saving power-consumption. The Architecture uses a CDAC to improve the linearity of 12 bit. Zhang, Dai, and Atila Alvand pour [12] describe a 14-bit 10-KS/s Successive-Approximation-Register which converts analog to digital form (ADC) for biomedical applications. A uniform geometry, a non-binary-weighted-capacitive digital-to-analog-converter is implemented to achieve enhanced linearity, and error correction is done using dynamically shift decision levels for the secondary-bit approach. Chen, C-H., Y. Zhang, J. L. Ceballos, and G. C. Temes. [13] Presented a SAR ADC Noise shaped with three capacitors. The literature proposes an effective SAR ADC. Application of oversampled schemes will achieve a high SNQR. In ultra-deep submicron CMOS technologies, the output of the proposed noise-formed ADC will be less degraded by the leakage current for low-frequency operation than for existing converters. C. Liu, S. Chang, G. Huang, and Y. Lin, [14]. A 10-bit 50-MS/s SAR ADC was constructed with Monotonic Capacitor Switching Procedure. High resolution converters are implemented using the cascaded/hybrid switching/ fully differential design with very high complex circuitry and large power consumption where a fully differential design is better in terms of complexity and speed

A completely differential ADC requires a larger capacitor array and typically consumes more space. Despite the fact that the unit capacitor size can be almost halved in fully-differential designs, the layout size of the dual capacitor array is typically larger, despite the fact that the dummy structures inside do not scale well with the unit capacitor size.

TABLE I. SUMMARY OF LITERATURE REVIEW

Reference Journals	[4]	[5]	[6]	[7]	[8]	[11]	[13]	[14]
Process Technology (nm)	28	90	180	130	55	55	55	55
DAC Architecture	Switched DAC	Capactive DAC	Switched DAC	Binary Weighted CDAC	Charge Sharing Capactive DAC	Split CDAC	CDAC	CDAC
Resolution (bits)	13	10	11	12	16	16	16	16
Sampling Rate (S/s)	500M	250M	2K	1K	1M	1M	1M	1M
Supply Voltage (V)	-	1.2	1.8	1	3.3	3.3	3.3	3.3
ENOB	-	8.645	10.14	10.47	-	-	-	-
FOM (fJ/conv)	3.83	77.3	120	76	0.126	0.126	0.126	0.126
SNR (dB)	63.74	-	62.8	64.8	100	100	100	100

There have been several methods offered to minimize the size of a standard fully-differential-capacitor array without using digital-calibration techniques [6, 13], but each has its own set of limitations. The size of the capacitor-array is reduced using the top-plate-sampling technique in [6]. As a result, the comparator's common mode is input dependent, and there's a chance of higher non-linearity errors.

The bottom-plate-sampling approach is kept while the array of capacitors is reduced to half its original size in [13]. Nonlinearity mistakes may occur as a result of the approach used. Although the completely differential topology has received a lot of attention in recent publications for various applications,

Due to the power and area limits for biomedical applications, the dual split capacitor DAC with differential sampling and single ended SAR ADC was chosen. Extra design time and energy are required to design and optimize for low power, hence a D flip-flop is utilized as a basic cell in the SAR logic. The only attractive choice for medium resolution and low power is the SAR ADC converters; these approaches provide better power efficiencies. The literature summary in Table-I shows that the proposed converters use conventional type of switching schemes to reduce the power consumption as with

different node technologies the switched CDAC is implemented but with increase in resolution and higher sampling rates the drawbacks are the achieved SNR is lower and figure of merit (FOM) is very low hence giving rise to nonlinearity of the converter which puts a limit on resolution and high speed of operation ,Several strategies have been applied to maximize the area and power efficiency in the suggested work, which focuses on a Dual split differential architecture with bootstrap sampling, in which multiple strategies have been used to optimize the area and power efficiency as follows:

A dual split capacitor DAC is developed for reduction in total area of the capacitance by more than 50% and a multiplier based switching is adopted for low power and also resulting in reduction in the switching energy.

- A preamplifier latch-based-comparator is designed and the circuit is controlled by asynchronous SAR logic for high speed and low dispersion delay with supply of 1V which eliminates external clock and also results in the optimized power of the comparator.
- To improve SNR an optimized bootstrap switch is used for sampling and using it in the differential mode with two complementary clocks for operation, a high speed, high SNR up to 80dB can be achieved.

The main goal of the proposed paper is to improve sampling rate higher than 100MS/s compared to the literature and to achieve further improvement in the SNR, ENOB, FOM and to present a DSATS-based DAC methodology to save switching energy and increase DAC linearity as compared to conventional architecture.

The objective of the proposed design is obtained from the literature summary and the specifications for the proposed design to meet the required resolution and 14-bit accuracy are addressed in Section II. Section III covers the ADC's sub-blocks, including bootstrap switching, the capacitive DAC's proposed design with multiplexer switching, and a preamplifier latch-based comparator with clock generating circuitry and SAR logic. Section IV discusses the complete integration of all the sub blocks. Section V discusses the proposed ADC structure's simulated measurement findings and, finally, the conclusion is presented in section VI.

III. SAR-ADC Key Building Blocks

The full SAR ADC architecture is depicted in Fig. 1 as a conceptual design. Differential sampling circuit, dual-split capacitor DAC design with switches, capacitors, voltage comparator and digital SAR logic are all part of it. This composition perfectly aligns the converter with the primary goal of optimizing the SAR logic and as a result, the converter's performance. The unit capacitance is 8fF is kept as tiny as possible to save space and switching energy with the total capacitance of DAC is roughly 824fF in this dual split DAC combination. Finally, the preamplifier latch-based voltage comparator is responsible for the SAR logic's operation. The inputs to SAR logic are driven to zero via a binary search at the start of conversion, and the input voltage is sampled on the capacitive DAC. The comparator makes its first judgment based on the polarity of the sampled output of the sampler, which reflects the most significant output bit (MSB). Depending on the result of this decision, to move the comparator input toward zero, the CDAC's greatest capacitance is switched. This process is repeated in smaller phases until all bits are resolved at the completion of the conversion, at which point the DAC output is valued. A small sampling capacitor is used for higher SNR and to achieve rail-to-rail signal swing. The complete design implementations of all the sub-modules are discussed in the next preceding sections

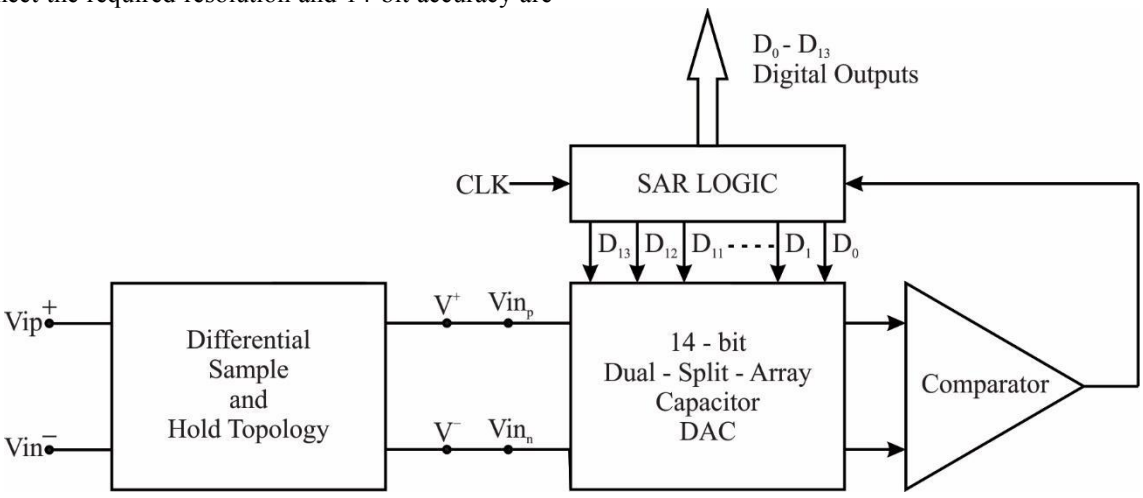


Fig. 1. Complete SAR ADC Architecture Built with Sub-Modules

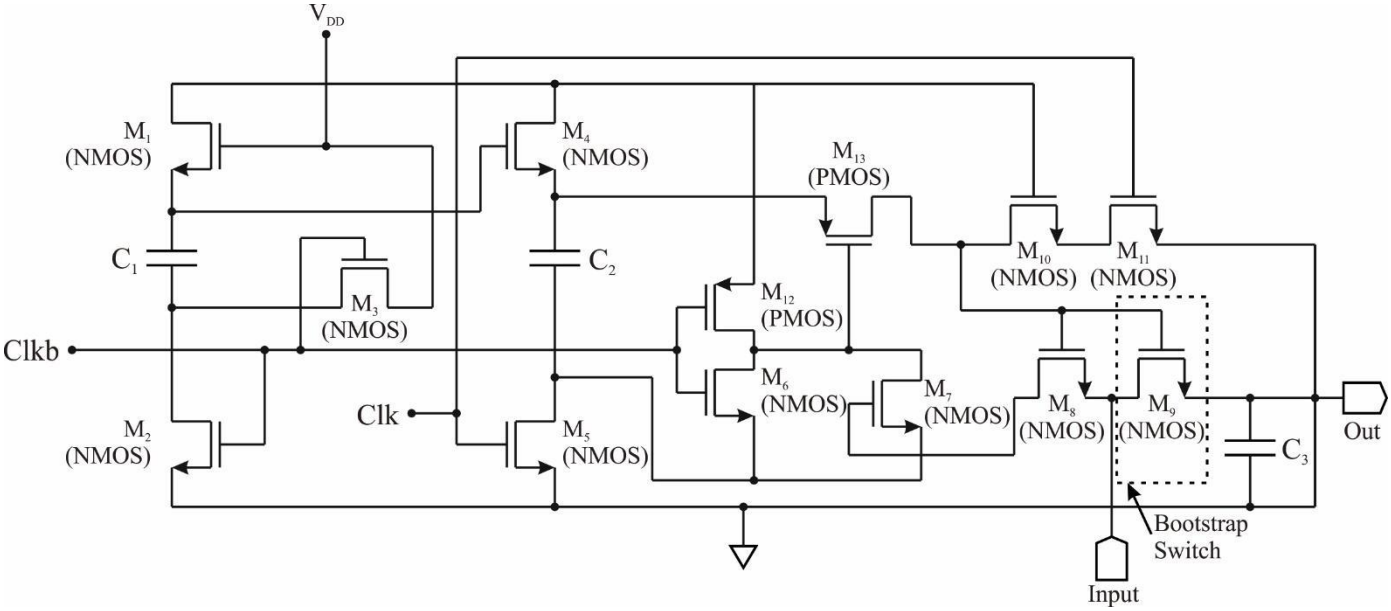


Fig. 2. Bootstrapped Switch

A. *Differential Sampling Circuit*

A fully differential architecture is one of the best methods to suppress supply noise and improve common-mode-noise-rejection and to achieve a 14-bit accuracy. The conventional Sample and hold (S/H) circuits were widely used for low-resolution data converters with resolution less than 8-bits and these conventional circuits [15] [16] suffer from many drawbacks like non-linearity, low speed, large capacitance. These circuits are seldom used in high-resolution, high-speed data converters. The proposed bootstrap topology has proven to be one of the best robust topologies for high speed, high resolution, and better linear characteristics.

B. *Design of Bootstrap Switch*

Bootstrapping switches are very power efficient due to the reason that there is no static power consumption while switching operation, and the parasitic body diodes on the chip are not active during the entire operation in sample and hold modes, bootstrapping switches are extremely energy efficient. The dynamic switching activity of the circuit is mostly responsible for the power loss in the bootstrap switch [17].

Fig. 2 shows the proposed bootstrap switch circuit, where the transistors M1-M5 are responsible for generating a gate voltage that is shifted by the NMOS transistor M8, C2, and the PMOS transistor M13 concerning the input voltage. When Clkb goes high, the NMOS M6 turns ON and applies the input voltage to the drain of PMOS M12, which drives the NMOS M7 to generate the sampled output voltage. The proposed design requires a single clock to attain a steady-state and the capacitors C1, C2, and C3 are charged to supply voltage at a steady state [18]. The charge across the output capacitor C3 is not larger than the supply voltage, so the driving voltage for the transistor switch does not exceed the supply voltage. The bootstrap switch samples the input voltage up to the supply voltage. With the bootstrapped switch M9, the gate-source voltage of the sampling transistor M8 is fixed at the supply voltage, resulting in a smaller constant on-resistance and better switch linearity. The dimensions of transistors $(W/L)p$ and $(W/L)n$ are the default values that are available in gpdk 90nm CMOS technology in the cadence virtuoso schematic editor tool. The design value of NMOS and PMOS is given in Table II.

TABLE II. DESIGN VALUES FOR BOOTSTRAP SWITCH

Parameters	Value
PMOS: $(W/L)_{1,2,3}$	1.2
NMOS: $(W/L)_{1,2,3,4,5,6,7,8,9,10}$	1.2

Fig. 3 shows the simulation characteristics of the proposed Bootstrap Switch. The proposed bootstrap topology samples the input signal at 10MHz frequency, with a sampling clock rate of 125MS/s i.e. at 8ns of the clock period, the sampling voltage range varies from 1mV to a maximum of 1000mV without any distortion at an output voltage as shown in Fig. 3

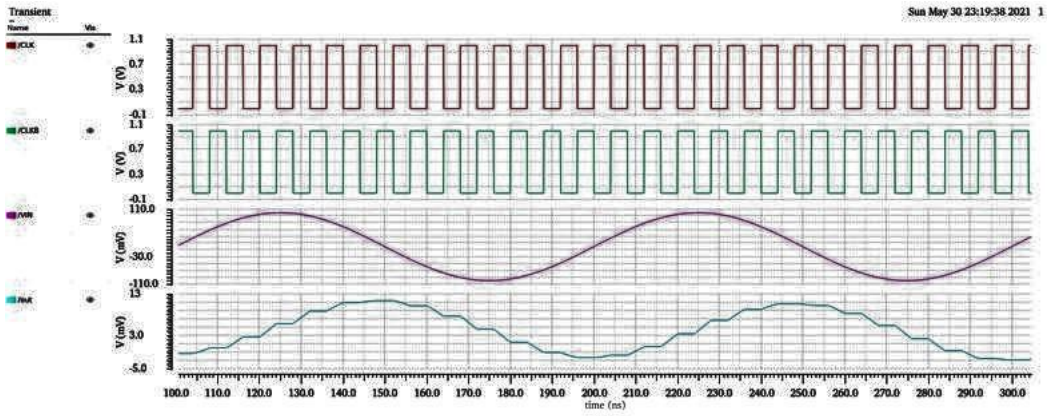


Fig. 3. Simulation Characteristics of Proposed Bootstrapped Switch

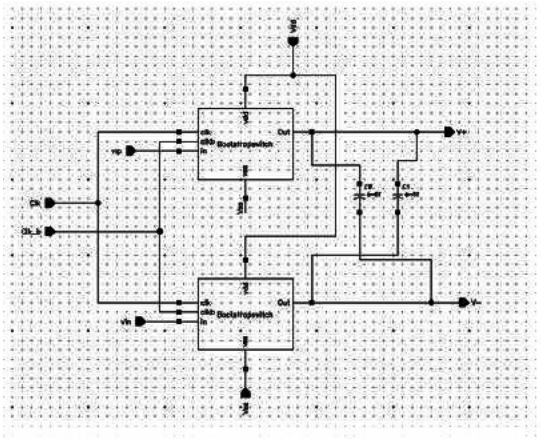


Fig. 4. Proposed Differential Samples and Hold Topology

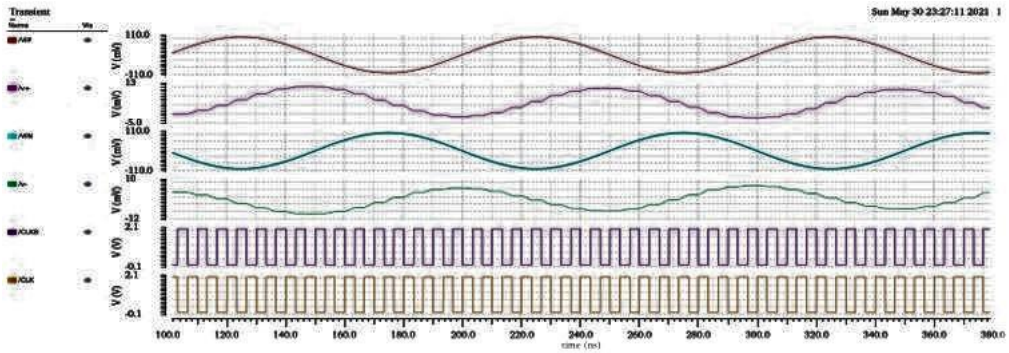


Fig. 5. Simulation Characteristics of Differential Sample and Hold Topology

C. Proposed Differential Sample and Hold Topology

The proposed bootstrap switch in section 3.2.1 is used to develop a differential [19] topology by arranging in differential mode as shown in Fig. 4, the two bootstrap switches are coupled using cross coupling capacitors to generate the differential output, When the bootstrapped switch is turned off, the input signal couples with the sampling capacitors via the Cds formed by the sampling transistor M8 the MOS drain-source capacitor and the routing parasitic capacitance. This coupling effect [20][21][22] corrupts the high-frequency execution, due to the unequal charges generated by Cds , resulting in a complex offset, to further reduce these adverse effects the capacitors are cross-coupled at the output of differential sample & hold topology.

The proposed differential sample and hold [23] topology is simulated with an input signal of 10MHz frequency, with sampling complimentary clocks at 125MS/s and simulated with the complimentary sampling input voltages [19] [22] varying between 1mV to a maximum of 1000mV as shown in Fig. 5, the complementary output obtained are digitized version of input signal with an advantage that there is a reduction in distortion and improved SNR compared to single-ended type topologies.

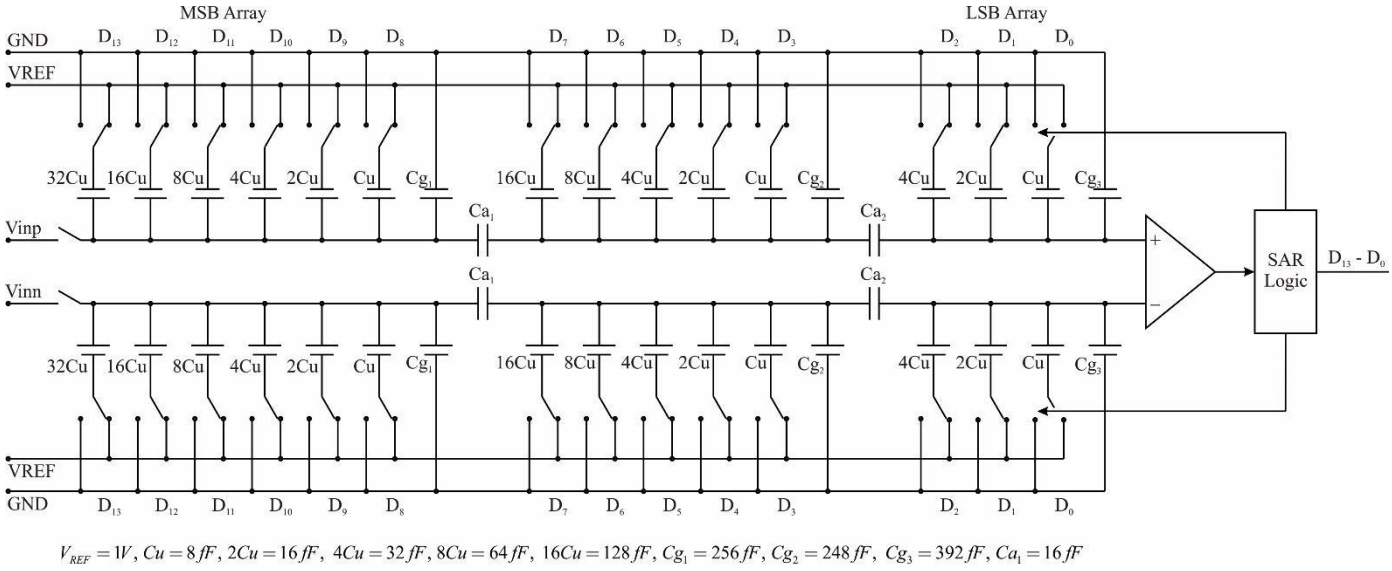


Fig. 6. Complete 14-bit Dual Split Capacitor DAC Architecture Circuit

D. Dual-Split-Capacitor-based-DAC Design Structure (DSC-DAC)

In the conventional design and development phase of any SAR ADC [24] the crucial building block is the DAC architecture, which has the greater importance compared to other building blocks due to the reason that the major area and power consumption in an ADC is because of the DAC module. Hence the total area and the power consumption is taken care by optimizing the design to the great extent. The main source of energy consumption in the capacitive DAC is during charging, therefore understanding the capacitor architecture is very vital. In a conventional binary-weighted capacitive DAC, the number of capacitors [25] required and the area occupied is very large, if the required resolution is 14 bits, in such cases, the MSB capacitor needs to be 214 Cu, where Cu is unit capacitor then MSB capacitor will have a larger value in the Pico- farad range thus occupying large area and power, to overcome such disadvantage the split architecture is proposed. To achieve a 14- bit accuracy, to suppress supply-noise and improve common-mode-noise-rejection a fully-differential (DSATS -DAC) architecture is proposed. Where the MSB capacitor required is 25 Cu, with the measure of MSB capacitance being 256fF which is very small compared to the conventional architecture, saving a large amount of area.

The proposed DAC architecture is a modified version of a conventional single split capacitor DAC architecture called dual split capacitor DAC that eventually reduces the total area capacitance by 99%. The existing DAC architectures for low power applications are capacitor-based DAC architecture which are better due to the zero quiescent current and capacitor mismatch required are very less compared to resistor type DAC structures [26] [27]. The matching requirements can be further reduced using complex digital circuitry, these complexities can be further reduced with improved speed performance by proposing the dual split array architecture with Ca1 and Ca2 as shown in Fig. 6. The proposed design of using the dual split capacitor DAC architecture is shown in Fig. 6.

In this research work, the capacitor array is divided into two separate arrays [28] and three segments, L, M, and N, with lengths 6, 5, and 3 that satisfy the required resolution as shown in fig.6. Let us consider Ca1 and Ca2 to be the two split capacitors with ground capacitances Cg3 and Cg2 and these capacitances can be evaluated considering the expression (1) and (2), where m and n are the length of the sections. Q is the least value of the capacitor ratio in the adjacent section, i.e $Q = 1$. Cu is the unit capacitance. The unit capacitance Cu is calculated by considering the sampling rate as 125 MS/s with $N = 14$ bit resolution, few of the possible significant combinations of L, M, N segments can be depicted using expressions (3), (4), (5), (6).

$$\frac{c_{g3}}{c_u} = \left(\frac{2^m - 1}{Q}\right) * \left(\frac{c_{a2}}{c_u}\right) - 2^m - 1 \quad \square\square\square$$

$$\frac{c_{g2}}{c_u} = \left(\frac{2^n - 1}{Q}\right) * \left(\frac{c_{a1}}{c_u}\right) - 2^m - 1 \quad \square\square\square$$

Considering

$$\frac{c_{a1}}{c_u} = w, \frac{c_{b2}}{c_u} = x, \frac{c_{a2}}{c_u} = y, \frac{c_{b3}}{c_u} = z \quad \square\square\square$$

$$y = 2^m \quad \square\square\square$$

$$z = \frac{4^m}{Q} - 2^{m+1} + 1 \quad \square\square\square$$

$$x = \frac{\left(2^n - Q\right) * w}{Q} - \left(2^n - 1\right) * Q \quad \square\square\square$$

With resolution of 14 bits, capacitors are divided into the segments with length $L = 6$, $M = 5$ and $N = 3$, The capacitor ratio is taken as unity. With these considerations, the total capacitance obtained for DSATS-CDAC is 824fF, with unit capacitance calculated to be 8fF, whereas for conventional binary weighted CDAC, it is 824pF, saving large amount of area around 90%, the switching energy for the proposed design is 8fJ whereas for the conventional binary weighted CDAC it is 50fJ for the same specification, these values illustrate that the proposed DAC is energy and area efficient. The operation of differential DSATS-CDAC consists of two sections namely the upper section and the lower section, when vinp, vinn is applied to the bootstrap circuit the sampled signal serves as the input on to the upper DSATS-CDAC top plate, whereas the bottom plate is reset to VREF. The comparator now performs comparison at its inputs, MSB bit in the SAR register is set then 32Cu is connected to GND, similarly the operation is repeated by connecting 16Cu to VREF and the cycle is repeated until the LSB bit is decided and all the 14-bits are set/reset in SAR register. This sort of DAC operation is referred to as monotonic since only one capacitor switch is used for each bit cycle, reducing charge transfer and resulting in lower power dissipation [29].

E. Switching Comparator Design

The comparator plays an important role in decision making and its switching function is the limiting component in high-speed data converter design, due to its power consumption, accuracy, and comparison speed [30]. The design of the comparator is a part of the complete system and is analog in nature. Comparator is one of the critical components in the implementation of the Successive Approximation Register ADC which is responsible for the conversion speed [31]. Because of its finite precision, comparison speed, and power consumption, the comparator is critical in the design of a high-speed data conversion system.

In the proposed work, for a 14bit SAR ADC, a preamplifier latch-based comparator is proposed that suits the basic requirements as it allows high-speed and low-power-consumption as shown in Fig. 7. The MOS transistors M1-M5 constitute the pre-amplifier stage acting as input stage that amplifies the smallest analog signal that can be applied to comparator, where the NMOS transistor M5 acts as a bias transistor with W/L as 50(5µ/100n). The preamplifier circuit also acts as the current mirror circuit with two PMOS transistors M1 and M2 having an aspect ratio (W/L) of 3.6 (360n/100n), the NMOS transistors M3 and M4, with an aspect ratio (W/L) of 1.5 (150n/100n) is used to provide dc offset voltage. The MOS transistors M6 -M9 forms the latch stage which is responsible for decision making and generating the output. In the latch stage, the PMOS transistors M6 and M9 and the NMOS transistors M7 and M8 are connected in anti-parallel to reduce the MOS transistors secondary effects, with the aspect ratio of 1.5 (150n/100n). The output of the preamplifier is taken as an input to the second stage PMOS transistors and as the internal clock goes high the comparator operation is initiated.

The feedback from the latch stage to the preamplifier stage reduces the noise in the signal [32]. The output is then converted into a logical signal by the output buffer formed by the transistor M10-M14 with W/L of 1.5 (150n/100n), which further reduces the offset voltage. The final comparator output obtained is free from noise variations. The combined pre-amplifier and latch stage ensures the high-speed operation and low power dissipation [33]. The high precision and resolution is obtained due to the amplifier being able to reduce the offset voltage. Fig. 7. Shows the schematic view of the high-speed differential comparator design.

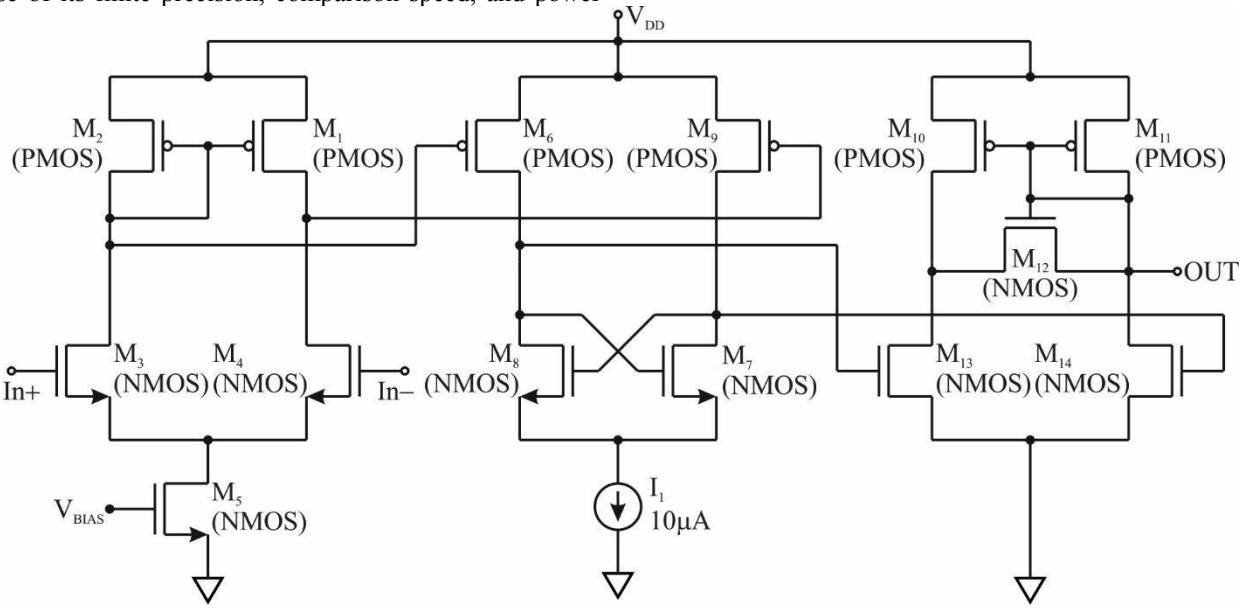


Fig. 7. Preamplifier Latch based Comparator Circuit

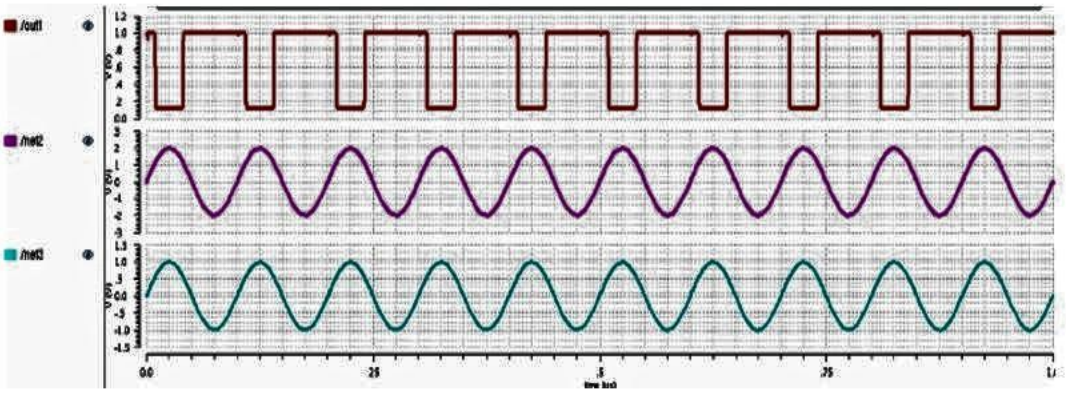


Fig. 8. Simulation Result of Preamplifier Latch Comparator

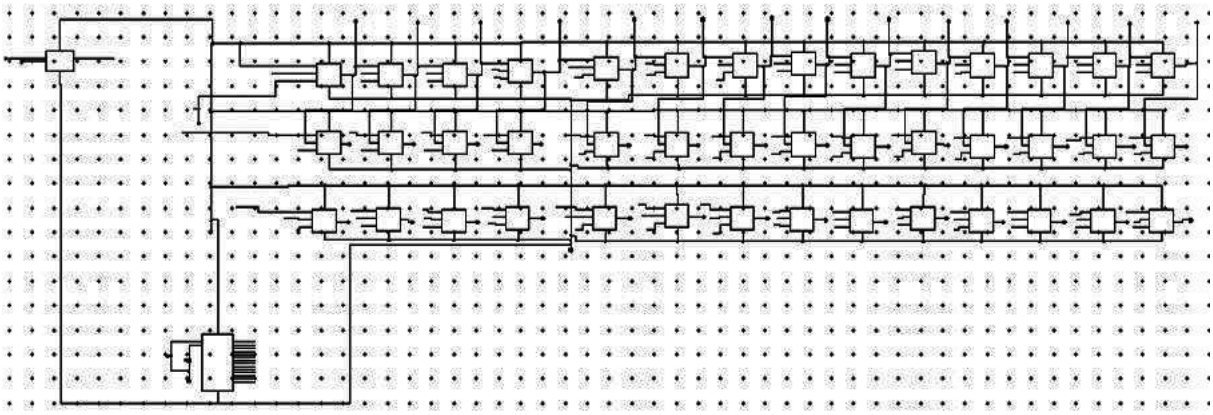


Fig. 9. Circuit Diagram of SAR Logic

The proposed preamplifier latch-based comparator with its simulation results for high-speed and low power-consumption are as shown in Fig. 8. The topology is simulated with a 1 V power supply and applied input sampling frequency of 10 MHz keeping Vbias = 0.5V and Ibias = 10μA. The simulation results of the propagation delay variation versus the input overdrive voltage with varying common-mode voltage are measured, as shown in Fig-8. With the simulated results it shows that the delay dispersions of the proposed comparator are 250ps.

F. The SAR Logic

The SAR logic block architecture is the core control circuit for the data converter as it is one of the most crucial decision blocks in making the complete logic system work. This logic block works similar to the digital weighing system, the output digital bits [23] for the applied analog input signal value and switching signals are sent to the DAC at proper intervals of time to obtain an approximated digital word within the conversion time of the converter. Successive registers use a binary search method with control logic for analog conversion [34]. DSATS-DAC samples the input signal at the start of the clock during the sampling phase. Based on the charges stored in the DAC, the differential input at the comparator switches to logic 1 or to logic 0. The change in the comparator inputs is due to the stored value and the approximated analog output of the DAC. The Successive register stores N bits of binary data for an N-bit converter based on the set/reset state of the register as shown in Fig. 9. The set bit can be a logic '1' whereas the reset is '0' or vice-versa. In the first stage of the 1st clock pulse, the rightmost register bit is set to '1' and other registers are reset to '0'. Similarly, the other N-1 bits of the N-bit converter are determined by a similar process. The process repeats for 14 clock cycles, at the end of the 14th cycle the approximated register holds the N-bit binary word. Thus, for an N-bit ADC N clock cycles are required to convert analog to digital word.

The NAND gates are utilized in conjunction with the D-flip-flop to supply the desired bit [35]. The chosen signal decides the DAC switch management signals and stores the output binary word through the Approximation registers as shown in Fig. 11. This kind of optimized SAR management logic makes single bit conversion easy without any additional delay [36] time between the latch comparator output and the DAC management signals, so that a better sample rate can be achieved. NAND gates and D-flip-flop are utilized to supply the sequence shifter. For low power converters the NAND gates are used to guarantee that one clock pulse is received by D-flip-flop as shown in Fig. 11(b).

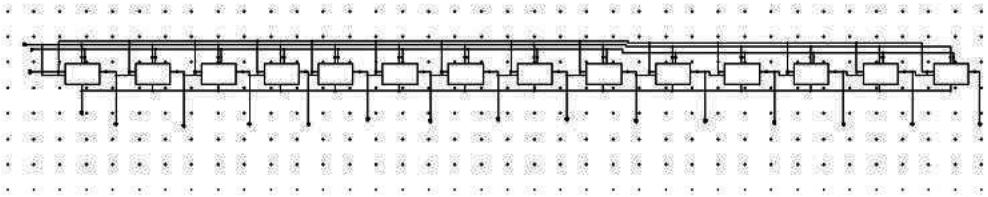
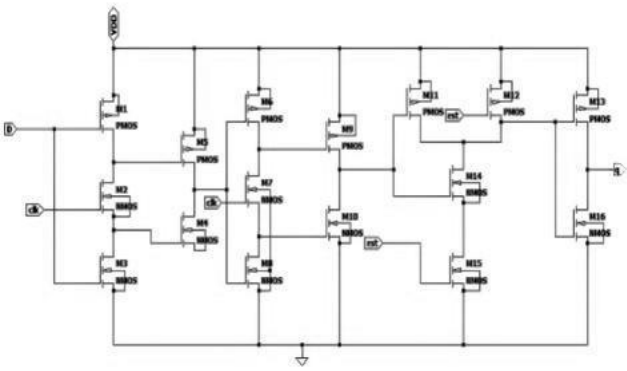


Fig. 10. Circuit Diagram of Clock Generation Circuit for SAR Logic



(a) Circuit Diagram of D Flip-Flop

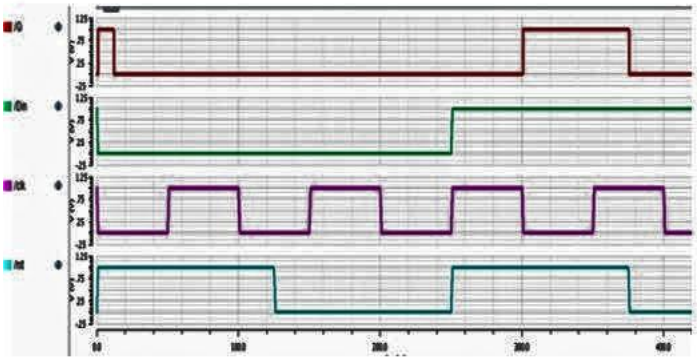


Fig. 11. (b) Transient Response of the D Flip-Flop

IV. Integration of 14-bit SAR ADC

The complete 14-bit SAR ADC is implemented using sub-modules as discussed in the previous sections and by aggregation of all the sub-modules a complete 14-bit SAR ADC is constructed. The complete VLSI design is implemented in 90nm CMOS technology as shown in Fig. 12. Using the Cadence EDA simulation environment for a confirmative block [37] level steady state analysis and verification using the long transient simulations are employed to characterize the parameters of the complete design module as shown in Fig. 13, the transient response in Fig. 13 shows during every clock cycle the SAR-register bits are set/reset and at the end of 14th clock, all the 14-word bits are available at the output [38] of the SAR. When the transient response progresses in time, there is an incremental shift in steps, which is the approximated digital output of proposed SAR [39] [40]. Analyzing the results obtained from the simulations, the key characteristic performance parameters are evaluated.

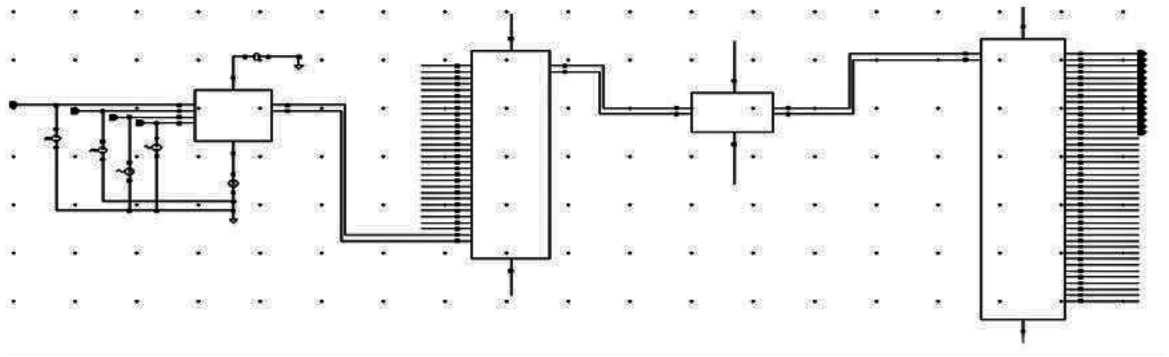


Fig. 12. Complete Schematic of 14-bit SAR ADC

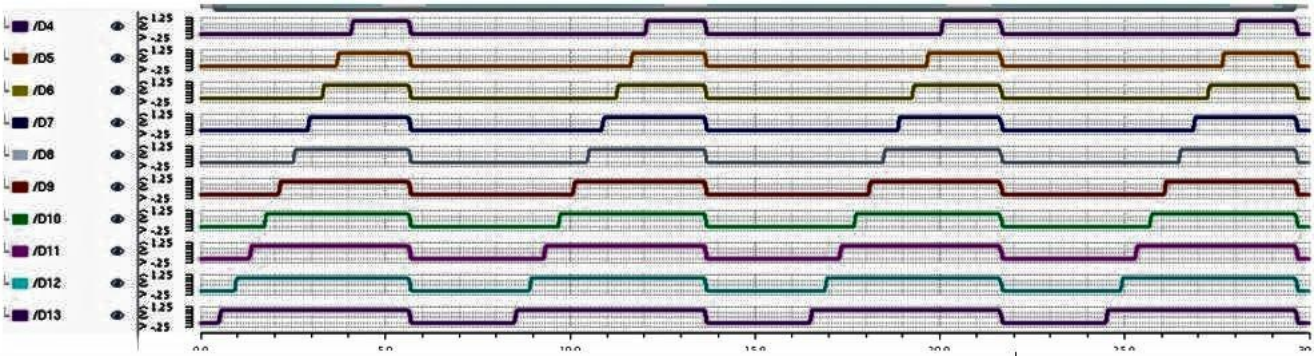


Fig. 13. Transient Response of 14-bit SAR ADC

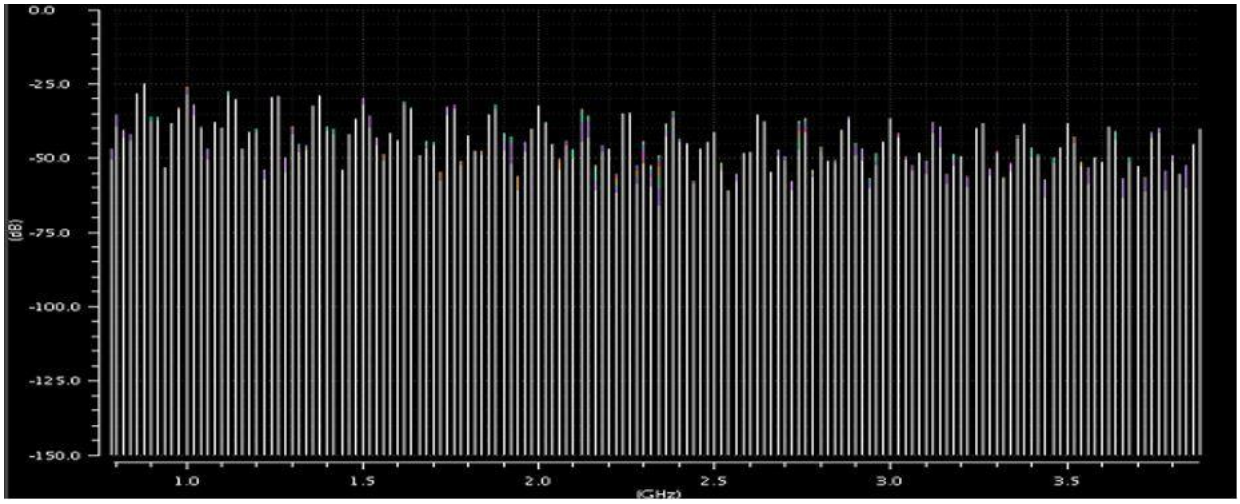


Fig. 14. FFT Spectrum of SAR ADC with 125MS/s Sampling Frequency

V. Results and Discussions

The proposed work includes the development of a Highly-Robust-Dual-Split-Array-Three-Section (DSATS) capacitor DAC (DSATS-CDAC), which addresses the need for a robust-DAC design for a stable and energy efficient SAR-ADC structure. The (DSATS-CDAC) architecture allows for two split segments, unlike typical capacitive DAC models. This is the only proposed ADC converter that uses an optimized DAC array in terms of unit capacitance to limit the effects of capacitive mismatch and parasitic capacitance, which reduces both energy consumption from 50fF to 8fF and the total capacitance of the DAC from 824pF to 824fF when compared to the conventional CDAC, which saves a large amount of area. The power consumption of the SAR-ADC is 42.8mW measured as a function of sampling rate, which ranged from 10MSps to 125MSps, with the supply voltage of 1 V. To run the simulation, the sampling rate was set to 125MSps, and the SAR - ADC input supply was set to 1 V. The switching energy consumed by the proposed DAC design is 8fJ. In addition, the comparator dispersion delay is as small as 250ps. The Fig. 14 shows the FFT-Spectrum at sampling frequency 125MSps with input sine wave for a frequency of 96 KHz. Table 4 summarizes the performance of the implemented SAR ADC converter when compared to contemporary state-of-the-art SAR-ADCs. With 90nm CMOS technology the sampling frequency is increased from 1kSps to 125MSps where the proposed ADC can be used

for high speed, with bootstrap and differential sampling there is a reduced distortion and improved SNR from 55dB to 81dB. DNL and INL in LSB as functions of the converter's output level code. For 14-bit resolution, The DNL measured at 125MSps is ±0.16 LSB, with an INL of ±0.16 LSB. The DNL/INL values are basically an indication of the performance related to the capacitance mismatch in the (DSATS-CDAC) architecture, the DNL/INL values obtained are less than 1LSB, and the proposed DAC can accurately resolve up to 13.16 bits for a proposed 14-bit resolution is one of the key achieved parameter. The figure of merit (FOM) of the proposed ADC is 37.3fJ/conversion-step at 125Ms/s and 1V supply which is better than other architectures as shown in Table III. The parameters obtained by the proposed converter are comparable to those obtained by previous medium-resolution converters.

TABLE III. COMPARISON WITH OTHER WORKS

	[30]	[7]	[15]	[24]	[25]	Proposed Work
Process Technology (nm)	65	130	180	90	65	90
Resolution (bits)	10	12	11	10	14	14
Sampling Rate (MS/s)	160M	1K	10K	100K	10K	125M
Supply Voltage (V)	1.2	1	0.75	1	0.8	1V
Power Consumption (W)	2m	110n	250n	0.5µ	1.98µ	42.82m
ENOB	8.9	10.47	9.76	8.5	12.5	13.16
FOM (fJ/conv)	25.4	76	28.8	9.76	34.2	37.43
SNR (dB)	55.6	64.8	60.5	-	77	81
DNL (LSB)	+0.47/-0.75	+0.35/-0.41	+0.6/-0.37	-	+2.28/-0.90	±0.16
INL (LSB)	+0.93/-0.97	+0.60/-0.74	+0.94/-0.89	-	+2.22/-2.26	±0.16

VI. CONCLUSION

A unique enhanced–linearity type 14-bit Asynchronous SAR ADC is suggested, featuring a low noise comparator with a switching latency of 250ps and differential sampling topology to improve SNR to 81dB and minimize the ADC's energy consumption. DSATS-CDAC is proposed with multiplexer-based switching to save 59.76% of the area and make the system more efficient. An improved SAR logic is also proposed to reduce the delay even further. The suggested ADC is simulated using a 90nm CMOS technology with a 1V supply, and the results show that it performs better than earlier approaches. Finally, the ADC achieves a sampling rate of 125MS/s with ENOB of 13.16, FOM of 37.43fJ/Conversion-step, and Differential and Integral nonlinearity of 0.16LSB. The efficient switching of the DSATS-CDAC suggests that the proposed ADC is monotonic with linear characteristics for a high resolution of 14 bits, based on these findings, the suggested ADC is appropriate for high-speed real-time and biomedical applications.

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1. Chaya Shetty M.tech student did the study on data converters and Designed SAR ADC converter and carried out simulation, executed and prepared original draft.
2. Dr. M. Nagabushanam has Designed the complete Architecture with specifications and derived (W/L) for the architecture in 90nm CMOS technology and is responsible for review and editing
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