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Fault Coexistence and Grading Aware TSV Test based on Delay Feature

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Abstract- Screening out the defects in the TSV manufacturing process and eliminating the resistive open fault and leakage fault as early as possible are beneficial to improve the yield and reliability of 3D ICs. The existing prebond test methods are confined to the test accuracy and detection range, especially the test confusion problem and the lack of diagnosable ability under the coexistence of multiple faults. Based on the fluctuation of delay feature caused by faults, a kind of fault coexistence and grading aware TSV test method is proposed to enhance the yield and reliability of TSVs in this paper. The reference TSV and the TSV under test are input with test stimuli simultaneously. Furthermore, the designed delay extraction circuit is utilized to generate the rising edge and the falling edge separately and additional fault grading circuit can be enriched according to the test requirements. Finally, a one bit comparator at the capture end is used to detect whether two pulse signals arrive simultaneously, so as to determine whether there is a fault and the type of fault. The simulation results indicate that the detection range of resistive open fault is more than 281 Ω, and the detection range of leakage fault is less than 223 $M\Omega$, which is better than most existing methods. While effectively solving resistive open fault and leakage fault, it can also successfully deal with the coexistence of two kinds of faults and achieve a 5-level fault grading ability with relatively low area overhead.

Keywords- Delay feature, fault coexistence, leakage fault, resistive open fault, through silicon via.

I. Introduction

THROUGH silicon vias (TSVs) based three dimensional integrated circuits (3D ICs) is characteristic of the smaller footprints, heterogeneous integration, higher performance and lower power consumption, which is essential to satisfy the strict requirement of the future application and the successful deployment of the technology [1] [2]. Despite the aforementioned advantages, yield and reliability have become the major concern of TSVs due to their vulnerability to thermal, stress, electron migration and defects brought in manufacturing process especially [3] [4] [5]. In order to address the above challenges and ensure the yield and reliability of 3D ICs, thorough detection of TSVs is particularly important [6].

Considerable built-in self-test (BIST) methods have been expended on detecting defects in a TSV by virtue of the intrinsic resistive or capacitive features of TSVs. As given in Table 1, the related test methods are detailed in terms of six features including the basic scheme, detection range of resistive open fault (R_{open}), detection range of leakage fault (R_{leak}), fault coexisting targeted, fault grade and area overhead.

A. *Test methods for resistive open fault or leakage fault*

Borrowing the wisdom of the IO-pin test, a leakage test and binning for TSVs is achieved by making the wait time of the CAF-WAS (Charge-and-float, wait-and-sample) method programmable via a dynamically tunable delay line, which is able to adapt to different user settings, such as different test thresholds and TSV sizes [7]. Unfortunately, this method cannot solve the resistive open fault. Another BIST methodology, architecture and circuits for testing prebond TSV is proposed to enhance 3D ICs yield and decrease overall test cost [8]. A scan switch network architecture is designed to carry out prebond TSV scan testing in test mode and operate as functional circuit in functional mode respectively. However, this method can only deal with the leakage fault and the area overhead is relatively large.

Based on a simple unbalanced circuit to compare the behavior of the TSV under test with the reference one, a BIST method is proposed to detect weak open and bridging defects [9]. Similarly, aiming to the resistive open fault, variation in the duty cycle of test stimulus after unbalanced logic gates are used to detect weak open defects in a TSV [10]. These two methods are suitable for the detection of resistive open fault, but they are not enough to detect leakage fault or fault coexisting.

B. *Test methods for both resistive open fault and leakage fault*

A versatile prebond TSV test method applicable before wafer thinning is presented to handle both the resistive open fault and leakage fault with the capability

Table 1: Comparison of existing BIST methods for TSV test

Research work	Basic scheme	R_{open}	R_{leak}	Fault coexisting	Fault grade	Area (μm^2)
2013-TCAD [7]	CAF-WAS	No	$62.5K\Omega - 8M\Omega^*$	No	Yes	54.43
2015-TCASI [8]	Path delay	No	$0.57K\Omega - 10K\Omega$	No	No	~ 100
2016-TVLSI [9]	Unbalancing circuit	$> 1K\Omega$	No	No	No	32
2019-TVLSI [10]	Duty cycle	$> 550\Omega$	No	No	No	11.72
2013-TCAD [11]	Ring oscillator	$100\Omega - 100K\Omega$	$20 - 500u\Omega^{-1***}$	No	No	49
2015-ITC [12]	Ring oscillator	$0.5K\Omega - 5K\Omega$	$2.5K\Omega - 20K\Omega$	No	No	20
2015-VTS [13]	Pulse shrinkage	$> 200\Omega$	$< 40M\Omega$	No	Excellent	75.54
2019-TVLSI [14]	Pulse shrinkage	$0.9K\Omega - 20K\Omega$	$3K\Omega - 40K\Omega$	No	Excellent	15.18
2018-ITC [15]	CP-PC	$0 - 30K\Omega$	$50K\Omega - 5M\Omega$	Mentioned	No	6.82-7.31
2019-TVLSI [16]	Switched capacitor	several $K\Omega$ level	$< 1000K\Omega$	No	No	6.73
2020-TCAD [17]	Switched capacitor	$> 300\Omega$	$615-829u\Omega^{-1***}$	No	No	43.72
2021-ACCESS [18]	Schmitt trigger	Yes	Yes	Yes	No	8.78
This work	Delay feature	$\geq 281\Omega$	$\leq 223M\Omega$	Yes	5-level	18.89-33.78

* The equivalent resistance of leakage fault is obtained when $V_{DD} = 1V$ and leakage current is $0.125uA - 16uA$.
** The area overhead is estimated by the 90 nm technology node, which is not converted to 45 nm due to the lack of specific units.
*** Here the leakage fault is given in the form of conductance according to the original.

to measure the severity of the fault [11]. A loop-back ring oscillator test structure combined with input sensitivity analysis is used to prove that the resistive open fault and the leakage fault affect a TSV measurable oscillation period in opposite ways. TSVs are utilized as capacitive loads of their driving gates in another ring oscillator based scheme. Resistive open fault and leakage fault can be detected separately by measuring the variations in resistive and capacitive (RC) parameters [12]. The limitation of these methods is that it cannot handle the problem of fault coexistence and the ability of fault classification.

In the pulse shrinkage based test, the rising and falling delay are converted into pulse width, and the pulse shrinkage technique is utilized to digitize the pulse width into a digital code which will be compared with an expected value of fault free [13] [14]. The advantage of this method is that the quantized digital code has the natural and excellent ability of fault classification, but like most existing methods, it is insufficient to deal with the coexistence of both faults.

Recently, based on the principle of a charge-pump and pulse-counting approach (CP-PC), a no-touch TSV test method is proposed to deal with the open and leakage faults with the quality of process corners, supply voltage and temperature (PVT) robustness [15]. The virtue of this method is that it can detect resistive open fault and leakage fault with less area overhead. However, the fault coexistence and fault grading are ignored.

Recent effort has been focused on the switched-capacitor based scheme. A prebond TSV test scheme with easily applied design for testability (DfT) architectures and a simple fault detection process is presented to detect open fault, leakage fault and high resistance fault [16]. More recently, since the TSV defect will lead to the variation of the resistive, conductive and capacitive (RGC) parameters, a post-bond TSV test method is proposed to measure the parameters so as to determine whether the TSV is faulty or not [17]. However, the two methods do not consider the coexistence or the classification of faults.

C. *Test methods for resistive open fault and leakage fault coexisting*

Although the problem of fault coexistence is mentioned in [15], no specific test method is given. Recently, a test method using Schmitt trigger (ST) as a TSV receiver is proposed to enhance test resolution and reduce test confusion when two kinds of faults exist simultaneously [18] [19]. Schmitt trigger that is characteristic of two threshold voltages is utilized to enhance the test resolution. By decreasing the supply voltage and discriminating whether the ring oscillator oscillates or not, it can identify whether there are two kinds of faults coexisting simultaneously. However, the disadvantage of this method is that it is only suitable for the test scheme based on ring oscillator, and it does not have the ability of fault grading. However, the limitation of this method is that it is only suitable for the test scheme based on ring oscillator, and it does not have the ability of fault grading.

D. *Motivation and technical contribution*

In general, the existing methods have advantages and disadvantages in terms of testing flexibility, detection range, test accuracy and area overhead. Through Table 1, we can find that the limitation of the above method is mainly embodied in three aspects. Firstly, the existing methods can basically solve one or two kinds of resistive open fault or leakage fault, but the largest limitation is that the coexistence of two kinds of faults is ignored. Secondly, most of the methods do not support fault classification, which lead to the insufficiency in the design for diagnosability. At last, the test cost of some methods,

such as area overhead is relatively large.

The coexistence of resistive open fault and leakage fault may be divided into the following three cases: 1) resistive open fault is stronger than leakage fault, and TSV presents a weaker resistive open fault. 2) The leakage fault is stronger than the resistive open fault. In this case, the TSV exhibits a weaker leakage fault. In both cases above, higher test accuracy or resolution is required, which will increase the difficulty and cost of the test. 3) Resistive open fault is approximately equal to leakage fault. At this time, the two kinds of fault effects cancel each other, which show as pseudo "fault free", leading to test confusion.

Furthermore, most method mentioned above can detect the type of fault exists in a TSV, but cannot evaluate the severity of the fault. On one hand, from the perspective of design for testability, the main criteria to measure the quality of test methods are test accuracy, fault detection range and flexibility of test methods. On the other hand, from the perspective of TSV manufacturer, the most favorable test result is to offer quality grading directly. Quality grading can provide classification according to the quality of TSV, and then it can be used in circuits with different accuracy requirements to reduce waste and manufacturing cost.

At present, there is no exact data on TSV yield in the academic or industrial circles, and there is no relevant report from the company about the probability of the coexistence of the two kinds of faults, but the possibility of the coexistence cannot be ruled out in theory. Especially, when testing a set of TSVs in parallel, for example, testing six TSVs in a group at the same time, it is possible that one TSV may exist resistive open fault while the other one may be leakage fault. Because the existing BIST methods are confined to the test resolution, it is likely to lead to inaccurate or even wrong results.

When both resistive open fault and leakage fault exist simultaneously, the fault effects caused by propagation delay cancel each other, which lead to test confusion and increase the difficulty of test. Different from the existing method based on the principle of propagation delay, the transition delay which is more sensitive to faults is used in this paper to solve the problem of two kinds of faults coexisting, so as to further improve the yield and reliability of TSVs. Firstly, the test stimulus is fed into the reference TSV and the TSV to be tested simultaneously. Secondly, the rising edge pulse or falling edge pulse is generated right after the designed transition delay extraction circuit according to the type of the fault to be tested. Moreover, additional fault classification circuit can be added to achieve a 5-level fault classification capability according to the test requirements in practical. At last, a one bit comparator at the capture end is utilized to detect whether the two pulse signals arrive at the same time. The technical merits of this method lie in the following four aspects.

- Different from [7]- [10], which can detect only one kind of fault, the scheme proposed can detect both resistive open fault and leakage fault successfully. Meanwhile, the rising edge delay and falling edge delay are extracted respectively to separate the mutual cancelation effect of them on the test results, so as to further solve the test confusion issue under the condition of fault coexisting that has not been properly solved in the existing solutions [7]- [17].

- Unlike [8]- [12], [15]- [18], this method can not only judge whether a TSV is faulty, but also diagnose the severity of the fault, and provide a quantitative 5-level classification result. This is conducive to reducing the waste of TSVs and reducing the total cost for products with different quality requirements.

- Compared with most of the existing methods, the detection range of this method is much wider. The detection range of resistive open fault is more than 281 Ω, which is better than most methods except [11], [13] and [15]. Meanwhile, the detection range of leakage fault is less than 223 $M\Omega$, which is better than most schemes except [11] and [17].

- Last but not least, the area overhead is relatively small. The area overhead of the test structure is only 18.89 μm^2. When fault classification is considered, the area overhead increases to 33.78 μm^2. However, compared with existing methods [7], [8], [11], [13] and [17], the area overhead is still small and acceptable. Meanwhile, compared with the area overhead of a single TSV, it is almost negligible.

The rest of the paper will be organized as follows. Influence of TSV fault on delay is analyzed in section II and test scheme proposed is described in section III. Section IV elaborates the simulation results and analysis, and followed by conclusions in section V.

II. Influence of TSV fault on delay

A. *Charge and discharge process of TSV as capacitive load*

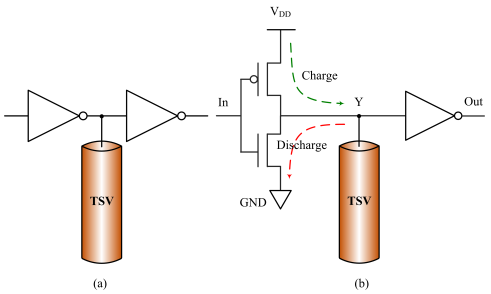

Fig. 1: Electrical model of TSVs before bonding.

The electrical model and fault model of a TSV, including diameter, height, oxide layer thickness, filling material, fault type and other parameters, have been introduced in detail in previous research work [18] [20] [21] [22]. On this basis, the charging and discharging process of TSV is further analyzed in this paper. The TSV with driver and receiver is shown in Fig. 1 (a). By converting the driver of TSV in Fig. 1 (a) from gate circuit to a

pair of PMOS transistor and NMOS transistor, Fig. 1 (b) can be obtained, and then the charging and discharging process of TSV can be analyzed as follows.

Firstly, when the input signal In is set to "0" long enough, the PMOS transistor turns on to charge the TSV. After charging, the top node of the TSV is Y ="1", and the output signal Out is "0". Secondly, when the input signal In is set to "1", the NMOS transistor is turned on to discharge the TSV. After a specific discharge time T, the TSV top node Y ="0" and the output signal Out ="1".

B. *Influence of TSV fault on delay feature*

The delay characteristics caused by TSV faults are summarized in Table 2. It can be found that the charging time (from "0"to "1") and the discharging time (from "1" to "0") become shorter when resistive open fault exists in a TSV. The reason is that TSV is divided into top capacitance dC and bottom capacitance $(1-d)\,C$ by the micro-void defect. The part near the top has powerful influence on the charging and discharging of TSV, and the bottom part has limited effect, where d represents the position of micro-void and C represents the parasitic capacitance of TSV. Therefore, compared with the TSV fault free, resistive open fault will result in the reduction of both rising edge and falling edge.

However, compared with resistive open fault, leakage fault exhibits different influences on TSV charging and discharging time. Because of the leakage resistance, the charging speed of TSV becomes slower. On the contrary, the discharging speed of TSV becomes faster. In other words, compared with the TSV fault free, the leakage fault will increase the rising edge time and decrease the falling edge time, and the overall propagation delay of the input signal is increased.

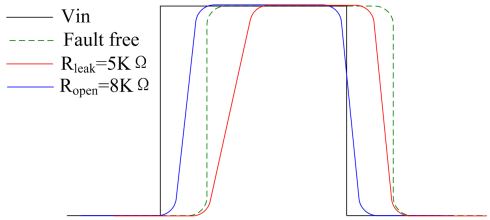

Fig. 2: Simulation waveform of delay caused by TSV fault.

Fig. 2 shows the simulation waveform of delay caused by TSV fault. The green dotted line and the blue solid line represent the delay of the TSV fault free and resistive open fault $R_{open} = 5K\Omega$ respectively. It can be seen that the rising time $\Delta tr = 48ps$ and the falling time $\Delta tf = 35ps$. Therefore, the pulse width is reduced by $\Delta tr - \Delta tf = 13ps$. However, when Δtr and Δtf decrease at the same time, the variation of final delay will be relatively weak or even negligible.

The red solid line shows the simulation waveform when the leakage fault $R_{leak} = 3K\Omega$. It is obvious that the rising time increases and the falling edge time decreases when leakage fault exists, which will lead to significant reduction of the overall delay.

Therefore, it can be concluded that when only considering the resistive open fault or leakage fault in a TSV, the type of fault can be judged by the fluctuation of the delay feature of the input signal. However, one of the disadvantages of this method is that its detection ability drops sharply when resistive open fault and leakage fault coexist. Through the above analysis, it can be found that the impact of resistive open fault and leakage fault on the falling edge is similar, that is both decrease, while the impact on the rising edge is opposite, which directly leads to the failure of all methods that do not separate the rising edge from the falling edge to test the two faults simultaneously. Therefore, for the test of multi fault coexistence, when the rising edge and the falling edge are separated, the result of the rising edge test is no longer reliable, but the result of the falling edge test can directly reflect the existence of multi fault.

III. Test scheme proposed

A. *Transition delay extraction circuit*

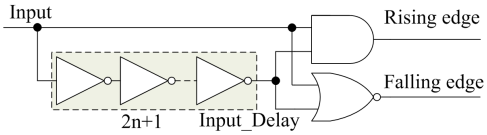

Fig. 3: Transition delay extraction circuit.

Fig. 3 shows the basic transition delay extraction circuit. A delay cell is constructed with $2n+1$ inverters, where n is equal to $0, 1, 2....$ The rising edge pulse is generated after signal $Input$ and signal $Input\_Delay$ pass through the AND gate, and the falling edge is generated after signal $Input$ and signal $Input\_Delay$ pass through NOR gate.

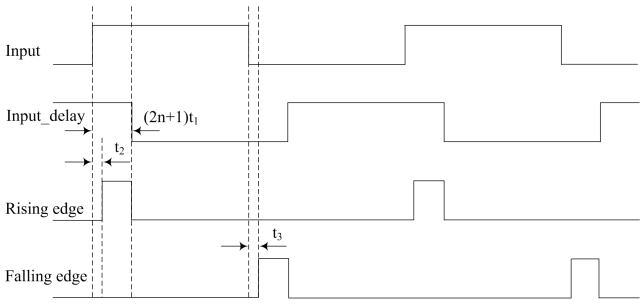

Fig. 4: Simulation waveform of transition delay extraction circuit.

Fig. 4 depicts the simulation waveform of the basic transition delay extraction circuit. If the gate delay time of a single inverter is t_1, the total delay time of odd number of $2n+1$ inverters will be $(2n+1)t_1$. Considering that the delay time of AND gate is t_2, and the delay time of NOR gate is t_3, so the pulse width of the rising edge is $(2n+1)t_1 - t_2$, and the pulse width of the falling edge is $(2n+1)t_1 - t_3$.

In the practical test process, the number of inverters in the delay chain should be adjusted according to

Table 2: Delay characteristics caused by TSV faults

Fault type	Charging time	Discharging time	Width of rising edge	Width of falling edge
Resistive open fault	↓	↓	↓	↓
Leakage fault	↑	↓	↑	↓

the counting frequency required by the counter or comparator and the estimated TSV fault severity, so as to determine an appropriate pulse width. The typical values of gate delay time of inverter are given in general manual. There are always some differences in gate delay time of actual devices, which can be determined by actual measurement.

B. TSV test architecture based on transition delay

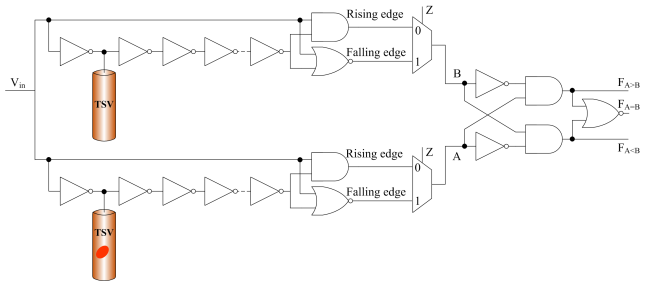

Fig. 5: TSV test architecture based on transition delay.

Fig. 5 shows the TSV test architecture based on transition delay. The principle of fault detection is as follows. The input signal passes through the reference TSV and the TSV to be tested respectively, and then, after the transition extraction circuit, the rising edge or the falling edge can be obtained. Finally, the comparator circuit judges whether the edge pulse arrives at the same time, and then determines whether there is a fault and which kind of fault.

The signal V_{in} at the input end is the test stimulus, and the common frequency range is $10MHz-100MHz$. The on-chip clock signal with similar frequency is also applicable. The detection end is composed of two transition delay extraction circuits to obtain the rising or falling edge of the reference TSV and the TSV to be measured respectively. According to the type of fault to be detected, the rising edge or falling edge is selected by the multiplexer, where $Z =$"0" means to extract the rising edge and $Z =$ "1" indicates to extract the falling edge.

The capture end is a two input comparator composed of two inverters, two AND gates and a NOR gate. The truth table of comparator is shown in Table 3. The logic functions of the comparator are as follows: 1) input node A is high level, and B is low level, output F means $A > B$; 2) input node A is low level, and B is high level, output F means $A < B$; 3) input nodes A and B are both low level or high level, output F means $A = B$.

Table 3: Truth table of one bit comparator

A	B	$F_{A>B}$	$F_{A<B}$	$F_{A=B}$
0	0	0	0	1
0	1	0	1	0
1	0	1	0	0
1	1	0	0	1

C. Test process

The test structure only needs one input signal V_{in} and 3 output signals. The test steps are as follows: 1) set the input V_{in} to the low level for a long time enough to charge the reference TSV and the TSV to be tested; 2) the input V_{in} is set to high level to discharge the reference TSV and the TSV to be tested; 3) observe the output combination of the output end to determine whether the TSV is faulty.

After finishing step 1, the voltage at both ends of A and B is low level. In step 2, both A and B will transit from low to high, but the fault severity will determine the time of transition. In step 3, the comparator can give the corresponding output results according to the sequence of A and B nodes transit from low level to high level.

The test stimulus V_{in} propagates along both the reference TSV and the TSV to be tested. When Z is set to "0", the rising edge variation is used for fault detection. Firstly, if $F_{A<B} = 1$ is captured, it means that compared with the reference TSV path, the charging time and rising edge time of TSV decrease after the input signal passes through the TSV to be tested, which means that there is a resistive open fault. Secondly, if $F_{A>B} = 1$ is captured, it indicates that the charging time and rising edge time of TSV are increased compared with the reference TSV path, which means that there is a leakage fault. At last, if $F_{A=B} = 1$ is captured, it can be further divided into two circumstances. 1) When only one type of fault is considered, such as resistive open fault or leakage fault only, it can be considered that the TSV under test is fault free. 2) When resistive open fault and leakage fault coexist, it can be considered that resistive open fault and leakage fault cancel each other. Further confirmation is needed and the specific method is detailed as follows. Set Z to "1", and use falling edge to detect. At this time, if $F_{A=B} = 1$ is captured, it is considered that there are resistive open fault and leakage fault coexisting.

It should be noted that although the falling edge narrowing feature can be used to detect whether there are

two types of faults, it is not recommended to do so directly. The reason is that, on one hand, when two kinds of faults coexist and the delay effect cancels out each other, the falling edge narrows slightly. Compared with the rising edge test, the falling edge has a smaller detection range and a larger error rate. On the other hand, in practice, the probability of resistive open fault and leakage fault has no detailed data, but it is far greater than the probability of coexistence of the two faults. Therefore, it is more pertinent to adopt the rising edge considering the probability of the fault targeted.

D. Fault grading circuit

The reference TSV is usually a fault free TSV with a driver and receiver. The fault free TSV can be considered as the capacitance between the TSV and the substrate, so the fault free TSV can be replaced by the reference capacitance C. It should be noted that after replacing the reference TSV with the reference capacitance C, the electrical parameters of the fault free TSV to be tested and the reference capacitance C are exactly the same, so the high-level signal of the input signal V_{in} will arrive at node A and node B at the same time, resulting in the uncertainty of the output result. In order to avoid the problem of output uncertainty caused by metastable state, the reference capacitance C is set to X times of the equivalent capacitance of fault free TSV, where X is close to 1 but less than 1, so that its delay time is infinitely close to but still less than the delay time of fault free TSV. For example, the equivalent capacitance of fault free TSV is 100 fF, the TSV delay time is 6.0 ns. If $X = 0.999$ is set, the reference capacitance C will be 99.9 fF and the delay time is 5.994 ns.

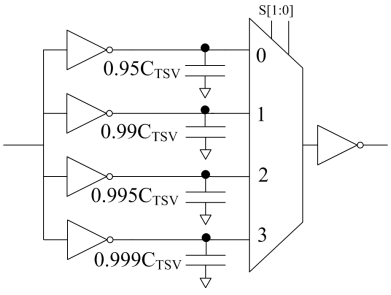

Fig. 6: Schematic of fault grading circuit.

Fig. 6 shows a detailed schematic of fault grading circuit. By adjusting the value of the reference capacitance C, the accuracy control of the fault grading structure can be obtained. The fault grading circuit is mainly realized by 1-of-4 multiplexers (MUX4), and the detailed structure will be given in section IV. The selection signal S is used to select the capacitance with different reference values, corresponding to the delay time of different reference TSV.

As shown in Table 4, the equivalent reference capacitance corresponding to the four combinations of S are $0.95C$, $0.99C$, $0.995C$ and $0.999C$ respectively. When the reference capacitance is $0.999C$, it is equivalent to Fig. 5. The test accuracy corresponding to the four reference capacitance values is low, medium, high and the highest, and the corresponding error rates are 5%, 1%, 0.50% and 0.10% respectively.

Table 4: Accuracy control of fault classification structure

$S[1:0]$	Reference capacitance	Test accuracy	Error rate
00	$0.95C$	Low	5%
01	$0.99C$	Medium	1%
10	$0.995C$	High	0.5%
11	$0.999C$	Highest	0.1%

E. TSV test structure with fault grading

Since the reference capacitance uses a MUX4, this will definitely increase the delay time of the reference TSV. In order to eliminate the increase of delay time caused by the MUX4, another MUX4 should be added to the TSV module under test. The TSV test structure with fault grading is depicted in Fig. 7.

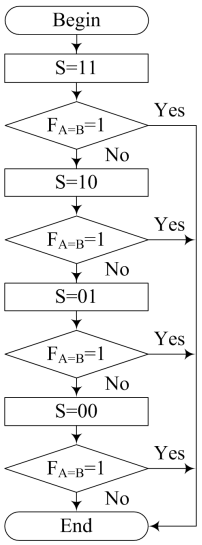

Fig. 8: Flow chart of fault grading.

As shown in Fig. 8, in the case of considering one single type of fault, the process of determining fault grading is as follows. 1) Set S to binary value "11", and select capacitance $0.999C$ through MUX4 for the first test. If the measurement result is no fault, the fault level is 0, and the test is terminated, indicating that the tested TSV is fault free, otherwise, the next step will be taken. 2) Set S to binary value "10", and select capacitance $0.995C$ through MUX4 and conduct the second test. If the test is passed, the test is terminated and the TSV fault level is 1. Otherwise, the next step will be shifted to. 3) Set S as binary value "01", and select capacitance $0.99C$ through MUX4 and conduct the third test. If the test is passed, the test is terminated and the fault level of TSV to be tested is 2. Otherwise, the next step will be carried out. 4) Set S as binary value "0", and select capacitance $0.95C$ through MUX4 and conduct the fourth

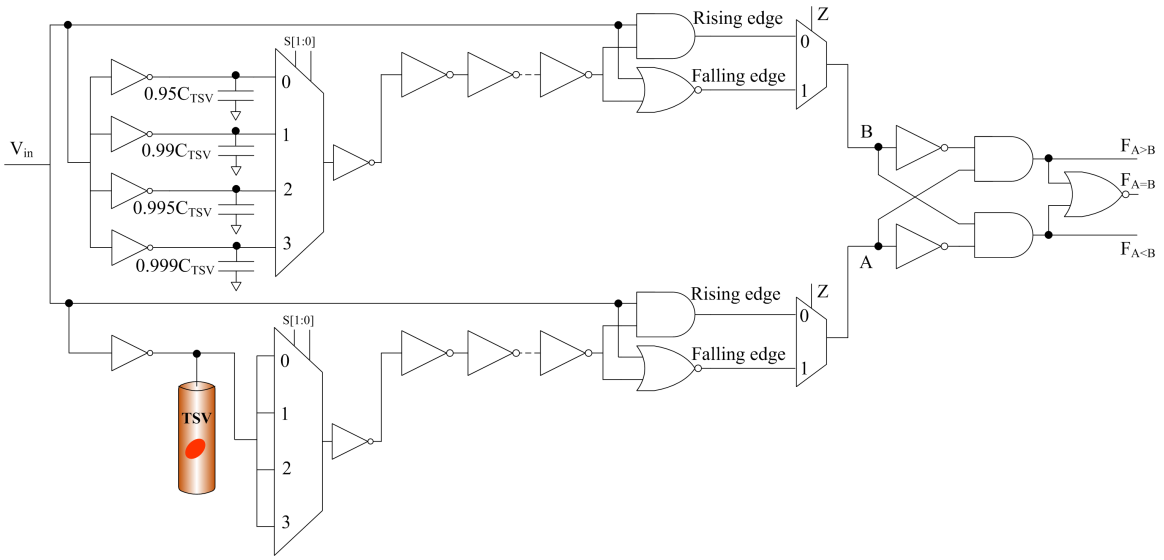

Fig. 7: Schematic of TSV test structure with fault grading.

test. If the test is passed, it indicates that the fault level of the tested TSV is 3; otherwise, it indicates that the fault level of the tested TSV is 4.

Obviously, the severity of the fault from light to heavy is $0 < 1 < 2 < 3 < 4$, the corresponding practical meaning is "fault free"<"slight fault"<"medium fault" <"serious fault" <"catastrophic fault". In addition, we note that it needs to be tested once in the best case and four times in the worst case. Although this is a serial test method, for TSV manufacturers, in order to reduce the test time, the fault severity of the same batch of TSV can be estimated, and the value of S can be set directly to skip some test steps. In general, it needs 2 or 3 tests to complete the whole fault grading process.

IV. Simulation result and analysis

In order to verify the feasibility and reliability of the proposed method, HSPICE is used to simulate in 45 nm process. The process model uses 45 nm PTM CMOS process [23] [24], the reference voltage V_{DD} is 1.1 V, and the equivalent capacitance C_{TSV} of fault free TSV is 59 fF. In the simulation, the position of resistive open fault is set in the middle of TSV, that is, $d = 0.5h$, where h is the height of TSV. For the sake of simplicity, the robustness of the proposed scheme to process variation is verified under various process corners of FF, FS, TT, SF and SS. The first letter represents the speed of NMOS, the second letter represents the speed of PMOS, F represents fast, S represents slow, and T represents typical.

A. Influence analysis of fault location

The leakage fault is mainly caused by the cracks on the side wall (S_iO_2) of a TSV during the manufacturing process. The size of the cracks determines the severity level of the leakage fault. Different from the leakage fault, the resistive open fault is due to the failure to completely remove the air during the copper filling process, which leads to the presence of micro-voids in the copper cylinder, or the misalignment between TSV and solder bump

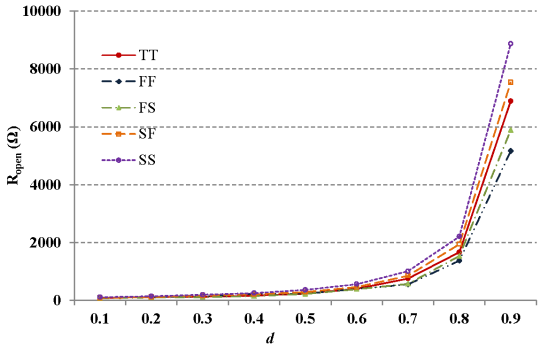

Fig. 9: Equivalent resistance of resistive open fault at different locations under process corners.

during the bonding process. In general, the equivalent resistance of resistive open fault is closely related to the position of micro-voids in copper cylinder. Fig. 9 depicts the simulation curves of fault location and equivalent resistance under different process corners, where the initial value of d is 0.1 and the step size is 0.1. The horizontal axis provides the location where the resistive open fault occurs, and the vertical axis represents the minimum resistance R_{open} that can be detected at this location. As can be seen from Fig. 9, the larger the d is, the larger the minimum R_{open} can be detected. For example, under TT process corner, the minimum detectable R_{open} is 281 Ω at $d = 0.5$, while the minimum detectable R_{open} is 130 Ω at $d = 0.2$, where the location of resistive open fault is closer to the bottom of TSV. In practice, a smaller R_{open} is usually more difficult to be detected, especially when it is close to fault free, and it is difficult to distinguish between the two. Therefore, it can be seen that the resistive open fault near the bottom of TSV is more difficult to detect. Moreover, there is a similar situation in other process corners.

B. *Detection range and grading for resistive open fault and leakage fault*

The equivalent resistance of the resistive open fault in the simulation is from 0 $K\Omega$ to 30 $K\Omega$, where 0 $K\Omega$ represents fault free and 30 $K\Omega$ means strong open fault, which is equivalent to the complete fracture of TSV in the middle position.

Regardless of fault classification, the equivalent resistance of the minimum resistive open fault that can be detected by this method is $R_{open} = 281\Omega$, that is, when $R_{open} > 281\Omega$ measured, TSV exhibits resistive open fault. Taken process variation into consideration, under the process corners FF, FS, SF and SS, the range of resistive open faults that can be detected are $R_{open} \geq 234\Omega$, $R_{open} \geq 225\Omega$, $R_{open} \geq 293\Omega$ and $R_{open} \geq 364\Omega$ respectively.

As far as leakage fault is concerned, only single leakage fault is considered, that is $R_{open} = 0$, $R_{leak} \neq \infty$. This method can detect the leakage fault in the case of equivalent resistance $R_{leak} \leq 223M\Omega$. Under the process corners FF, FS, SF and SS, the range of leakage faults that can be detected is $R_{leak} \leq 185M\Omega$, $R_{leak} \leq 230M\Omega$, $R_{leak} \leq 217M\Omega$ and $R_{leak} \leq 265M\Omega$ respectively.

Considering the fault classification, five resistive open faults and five leakage faults are injected respectively under single fault condition. The fault type, equivalent resistance, reference capacitance, results captured, corresponding fault levels and practical significance under various combinations are listed in Table 5.

For example, for the resistive open fault $R_{open} = 137\Omega$ injected, $F_{A=B} = 1$ indicates that although TSV is not in the ideal fault free state, it is still considered as fault free, and the corresponding fault level is 0. Under the conditions of $R_{open} = 1K\Omega$, $R_{open} = 2K\Omega$, $R_{open} = 10K\Omega$ and $R_{open} = 30K\Omega$, $F_{A<B} = 1$ shows that there are resistive open fault. The fault level is determined by the reference capacitance. According to the test flow depicted in Fig. 8, the corresponding fault level can be obtained. For example, at the time $C_{REF} = 0.999C$, if $F_{A<B} = 1$ is true, it indicates that there is no fault in the TSV and the fault level is 0; otherwise, if $C_{REF} = 0.995C$ is reset and $F_{A<B} = 1$ is true, the corresponding fault level is 1. The detailed equivalent resistance and fault classification are shown in Fig. 10. Using the test method similar to resistive open circuit fault, five leakage fault levels can be obtained.

Fig. 10 shows the equivalent resistance and fault classification of resistive open fault at the position $d = 0.5h$. The bars in the figure represent the minimum equivalent resistance R_{open} that can be detected under different reference capacitances. It is worth noting that the smaller the equivalent resistance of resistive open fault is, the more difficult it is to detect. When $R_{open} = 0\Omega$, TSV is in an ideal fault free state. Due to the limitation of the test resolution, when $C_{REF} = 0.999C$ is set, $F_{A=B} = 1$ is measured in the range of $R_{open} \leq 281\Omega$, indicating that the TSV under test is considered to be fault free and the fault grading is classified as 0, which

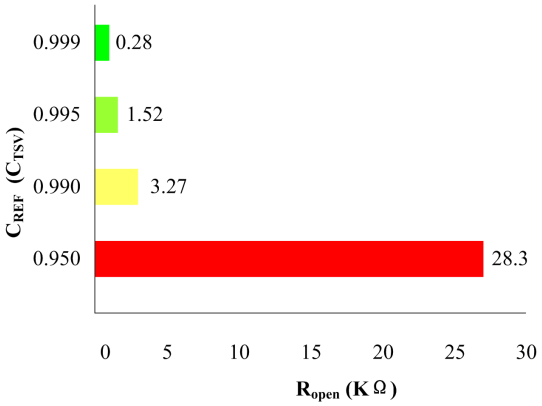

Fig. 10: The grading of resistive open fault.

shows that the minimum resistive open fault that can be detected by this scheme is 281Ω. Similarly, in the range of $281\Omega < R_{open} \leq 1.52K\Omega$, the fault grading of TSV to be tested is 1, which belongs to slight open fault. If $1.52K\Omega < R_{open} \leq 3.27K\Omega$ is true, the fault grading is 2, which belongs to medium open fault. If $3.27K\Omega < R_{open} \leq 28.3K\Omega$ is true, the fault grading is 3, which is a serious open fault. At last, if $R_{open} > 28.3K\Omega$ is true, the fault grading of TSV to be tested is 4, which classified as the highest level of catastrophic open fault.

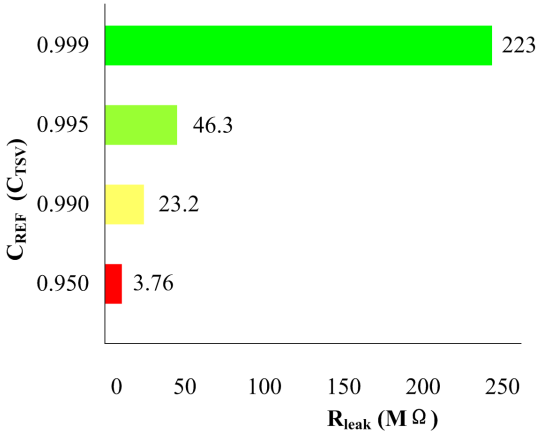

Fig. 11: The grading of leakage fault.

Similar to resistive open fault, the grading leakage fault can also be represented by bar graph. As shown in Fig. 11, each bar in the diagram represents the maximum equivalent resistance of leakage fault that can be detected under different reference capacitance. It should be noted that the larger the equivalent resistance of leakage fault is, the more difficult it is to detect. When $R_{leak} = \infty$, TSV is in an ideal fault free state. For example, in the simulation, when $R_{leak} \geq 223M\Omega$, the TSV to be tested is considered as fault free and the fault grading of leakage fault is classified as 0, which indicates that the maximum leakage fault that this scheme can detect is $223M\Omega$. If $46.3M\Omega \leq R_{leak} < 223M\Omega$, the fault grading of TSV to be tested is 1, which belongs to slight leakage fault. If $23.2M\Omega \leq R_{leak} < 46.3M\Omega$, the fault grading of TSV under test is 2, which belongs to medium leakage fault.

Table 5: Detection results and fault grading under various fault combinations

Fault type	Equivalent resistance	C_{REF}	Results captured	Fault level	Practical significance
Resistive open fault	$R_{open} = 137\Omega$	$0.999C$	$F_{A=B} = 1$	0	Fault free
	$R_{open} = 1K\Omega$	$0.995C$	$F_{A<B} = 1$	1	Slight open fault
	$R_{open} = 2K\Omega$	$0.99C$	$F_{A<B} = 1$	2	Medium open fault
	$R_{open} = 10K\Omega$	$0.95C$	$F_{A<B} = 1$	3	Serious open fault
	$R_{open} = 30K\Omega$	$0.95C$	$F_{A>B} = 1$	4	catastrophic open fault
Leakage fault	$R_{leak} = 300M\Omega$	$0.999C$	$F_{A=B} = 1$	0	Fault free
	$R_{leak} = 50M\Omega$	$0.995C$	$F_{A>B} = 1$	1	Slight leakage fault
	$R_{leak} = 30M\Omega$	$0.99C$	$F_{A>B} = 1$	2	Medium leakage fault
	$R_{leak} = 10M\Omega$	$0.95C$	$F_{A>B} = 1$	3	Serious leakage fault
	$R_{leak} = 3M\Omega$	$0.95C$	$F_{A<B} = 1$	4	catastrophic leakage fault

If $3.76M\Omega \leq R_{leak} < 23.2M\Omega$, the fault level of TSV to be tested is 3, which is a serious leakage fault. If $R_{leak} < 3.76M\Omega$, the fault level of TSV to be tested is 4, which belongs to catastrophic leakage fault.

C. *Analysis for resistive open fault and leakage fault coexisting*

In order to simplify the analysis, only one resistive open fault and one leakage fault are considered. Assuming that the resistive open fault occurs at the position $d = 0.5h$, the equivalent resistance of resistive open fault are injected under the conditions of $R_{open} = 1K\Omega$, $R_{open} = 2K\Omega$, $R_{open} = 10K\Omega$ and $R_{open} = 30K\Omega$ respectively, so as to determine the leakage fault range that can be detected under different fault levels. The detection range of leakage fault under specific resistive open fault considering fault coexisting are shown in Table 6. It can be seen from the table that after injecting leakage fault into TSV with resistive open fault, the fault grading is less than or equal to a single fault, and the fault level of TSV to be tested shows a downward trend. For example, if the injected fault is ($R_{open} = 0\Omega$, $R_{leak} = 30M\Omega$), where $R_{open} = 0\Omega$ represents there is no open fault. It can be seen from Fig. 11 that the fault level is 2, which belongs to medium leakage fault. However, when the injected fault combination is ($R_{open} = 2K\Omega$, $R_{leak} = 30M\Omega$), according to Table 6, the fault level is updated to 1, which belongs to slight fault. The reason lies in that under the condition of fault coexisting, the effects of resistive open fault and leakage fault on the charging and discharging time and delay time of TSV under test are mutually counteracted. Therefore, it appears to be a weaker resistive open fault or a weaker leakage fault.

However, under the condition of fault coexisting, although the fault level seems to decline, it is not true that the fault severity is reduced or there is no fault. On the contrary, the coexistence of faults increases the difficulty of detectability, and some false "weak faults" and "fault free" will threaten the product quality. At the same time, because it is masked by resistive open fault, the leakage fault which is difficult to detect will also increase the power consumption of 3D ICs.

Table 7: Area overhead of the proposed test architecture

General cell	Number	Area overhead (μm^2)
INV_X1	16	0.532
AND2_X1	4	1.064
NOR2_X1	3	0.798
MUX2_X1	2	1.862
Total Area (μm^2)		18.89

Table 8: Area overhead of test architecture considering fault grading

General cell	Number	Area overhead (μm^2)
INV_X1	19	0.532
AND2_X1	4	1.064
NOR2_X1	3	0.798
MUX2_X1	2	1.862
MUX4	2	6.65
Total Area (μm^2)		33.78

D. *Area overhead*

Without considering fault grading, the proposed test architecture consists of 16 inverters, 4 AND gates, 3 NOR gates and 2 multiplexers. All general cell, number and area overhead are listed in Table 7. The area overhead of a single standard cell is referred to Nangate 45 nm open cell library. As shown in Table 7, the total area overhead is 18.89 μm^2.

As listed in Table 8, additional three INV_X1 and two MUX4 are added considering fault grading. The total area overhead increases to 33.78 μm^2. It is worth reminding that MUX4 is not in Nangate 45 nm open cell library. Here, a common structure shown in Fig. 12 is adopted, which is composed of two INVs_ X1, three AND3_ X1 (1.330 μm^2), one OR4_X1 (1.596 μm^2), and the area overhead is 6.65 μm^2. In general, even considering the fault grading, the area overhead is still small, which is almost negligible compared with a TSV.

Table 6: Detection range of leakage fault under specific resistive open fault considering fault coexisting

level	$R_{open} = 1K\Omega$	$R_{open} = 2K\Omega$	$R_{open} = 10K\Omega$	$R_{open} = 30K\Omega$
Level 0	$R_{leak} \geq 158M\Omega$	$R_{leak} \geq 83M\Omega$	$R_{leak} \geq 16.5M\Omega$	$R_{leak} \geq 8.7M\Omega$
Level 1	$34.5M\Omega \leq R_{leak} < 158M\Omega$	$5.2M\Omega \leq R_{leak} < 83M\Omega$	$3.4M\Omega \leq R_{leak} < 16.5M\Omega$	$1.94M\Omega \leq R_{leak} < 8.7M\Omega$
Level 2	$4.8M\Omega < R_{leak} < 34.5M\Omega$	$2.3M\Omega \leq R_{leak} < 5.2M\Omega$	$0.82M\Omega \leq R_{leak} < 3.4M\Omega$	$0.47M\Omega \leq R_{leak} < 1.94M\Omega$
Level 3	$2.2M\Omega < R_{leak} < 4.8M\Omega$	$1.14M\Omega \leq R_{leak} < 2.3M\Omega$	$0.36M\Omega \leq R_{leak} < 0.82M\Omega$	$0.12M\Omega \leq R_{leak} < 0.47M\Omega$
Level 4	$0\Omega \leq R_{leak} < 2.2M\Omega$	$0\Omega \leq R_{leak} < 1.14M\Omega$	$0\Omega \leq R_{leak} < 0.36M\Omega$	$0\Omega \leq R_{leak} < 0.12M\Omega$

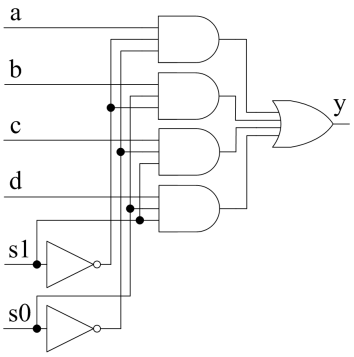

Fig. 12: Structure of MUX4.

V. Conclusion

Prebond TSV test is an important component of 3D ICs testing. It can eliminate the fault TSV in the earlier manufacturing process, effectively improve the yield of 3D ICs products and reduce the manufacturing cost. In this scheme, the rising edge and the falling edge are extracted separately to eliminate the interaction between them. This method can not only detect resistive open fault or leakage fault, but also solve the problem of test confusion when two kinds of faults coexist. The minimum resistive open fault detected by this scheme is 281Ω, and the weakest leakage fault is $223M\Omega$, which is better than the existing test scheme in terms of the detection range. Meanwhile, considering fault coexisting, a 5-level fault classification structure is proposed with area overhead of only $33.78\mu m^2$. Compared with the similar test methods, this scheme has very prominent advantages in the aspects of fault coexistence, detection range, area overhead and application scope of the method.

Conflict of interest

The authors declare that they have no competing financial interests or personal relationships that could have appeared to influence the work reported in this paper.

Author contributions

Chang Hao, Ni Tianming and Li Yang conceived and designed the experiments; Chang Hao, Xu Yong, Li Feng and Liang Houjun implemented the models, performed the experiments, analyzed the experiment data and wrote the paper; Xu Yong and Li Feng fine-tuned the paper and gave some precious advice.

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