FinFET based design and Performance Analysis of Nano-Processor for low area, low power and minimum delay using 32nm

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Abstract— The recent technologies in VLSI chips has grown in terms of scaling of transistor and device parameters but still there is a challenging task for controlling of current between source and drain terminals. For effective control of device current, the FinFET transistors have come into VLSI chip manufacturing, through which current can be effectively controlled. This section addresses the issues present in CMOS technology and majorly concentrated on proposed 4-bit Nano processor using FinFET 32nm technology by using Cadence Virtuoso software tool. In the proposed Nanoprocessor design, the first portion of the design is done using 4bit ALU which includes all basic and universal gates, high speed adder, multiplier and multiplexer. The Carry Save Adder (CSA) and multiplier are the major sub component which can optimize the power consumption and area reduction. The second portion of the proposed Nano processor design is 4-bit 6T SRAM and encoder and decoder and also using Artificial Neural Network (ANN). All these sub components are designed at analog transistors (Schematic level) through which the Graphic Data System (GDS-II) is generated through mask layout design. Finally, the verification and validation are done using DRC and LVS and at the last chip level circuit is generated for chip fabrication. The ALU is designed by using CMOS inverters and the designed ALU schematic is simulated through 32nm FinFET using technological library and compared with CMOS technology which is simulated through 32nm CMOS library (without FinFET). The power consumption of AND, OR, XOR, NOT, NAND gates, SRAM, Encoder, Decoder and ANN are 36.09nW, 64.970nW, 61.13nW, 33.31nW, 37.45nW, 32.5% with optimization in power dissipation of 47% along with optimization in leakage current, with 2.68uW, 1.98uW and 7.5% improvement in power consumption and 0.5% information loses are compressed subsequently respectively. The basic gates, universal gates, CSA, subtraction and MUX are integrated for 4-bit ALU design and its delay, power consumption and area are found to be 0.104nsec, 314.4uW and 56.8µsqm respectively.

Keywords—About four key words or phrases in alphabetical order, separated by commas.

I. INTRODUCTION

Rather than the dynamic force, static force from a transistor is devoured because of a little consistent release of current also called spillage. There are a few methods of spillage, however they can be extensively named as sub-edge, entryway and converse one-sided channel and-source substrate intersection band-to-band-burrowing (BTBT) [1, 2]. These spillage instruments have solid reliance with a few gadget parameters (e.g., oxide thickness, doping fixation, temperature), notwithstanding the flexibly and edge voltage of these gadgets. On account of these subsequent impacts, is done with the more testing to precisely evaluate transistor level patterns in static force [10]. In any case, the general static force because of spillage has been consistently becoming issue in the course of the last a few innovation ages [3]. Sub-limit spillage, which has an exponential reliance with the edge voltage, expanded quickly with the scaling of edge voltage and commonly overwhelmed the spillage flows [4]. The limit voltage has nearly little scaling to counter this sub-limit spillage, yet the scaling of other gadget parameters (e.g., oxide thickness) caused an ascent in door spillage and BTBT. In this manner, both these two spillages are presently used to establish a considerable division of the spillage [1]. Regardless of this consistent ascent, a few methods

have indicated huge potential in moderating the spillage (e.g., high-metal oxides, two fold door gadgets). Inside an innovation age, circuit planners pick the ideal methods for controlling the spillage vitality, dictated by the advancement of the general force execution of the framework [5]. The impact of door channel/source underlaps (Lun) on a thin band LNA execution has been contemplated, in 30 nm FinFET utilizing the gadget with blended mode recreations. Studies are done by keeping up and not keeping up the spillage current (Ioff) and edge voltage (Vth) of the different gadgets. To show signs of improvement commotion execution and addition, Lun in the scope of 3-5nm is suggested [13]. The structure of a chip must conjoin two key innovation patterns: i.e., to have drifts in semiconductor industry that underlies the fundamental structure square of microchips and to get patterns in programming that sudden spike in demand for these microchips [11]. The most significant pattern in the semiconductor innovation is the scaling of transistor gadgets, permitting to twofold the quantity of accessible transistors on a chip like clockwork [6]. Notwithstanding this exponential development in gadgets, the scaling additionally accompanies an improvement in the exhibition of every gadget, empowering all the more remarkable chip in progressive ages. Misusing the simultaneousness, and the calculation data transmission managed by these multicores is a significant plan challenge for the future frameworks, enveloping different layers of framework creators from the equipment modelers to the application engineers [9]. Then again, the predominant correspondence transmission capacity and inactivity between on-chip centers to have novel procedures to deal with the total access, in order to fulfill the interest for execution and vitality proficiency in the circuit. A large number of these strategies may have been altogether infeasible in multiprocessors worked from uniprocessor chips and subsequently neglected to legitimize genuine contemplations previously. One more test rotates around guaranteeing execution, particularly when the characteristic unwavering quality from the equipment segments is required to fall with the innovation scaling [10, 11]. A few current age multiprocessor chips are as of now working close to the building limit for power, in light of air cooling [12, 13]. With the exponential development of transistor gadgets, the capacity to put all the more handling centers on a chip is currently ready to effectively outpace the relating capacity to control up these centers at the same time.

Standard FinFET's properties are homogeneous to the planar technology, except it differs in its electrical performance and its arrangement of transistors. One or more FinFET fabric is the independent gate (IG) FinFET. Each independent gate is separately controlled by another. By employing the IG device, the probability of obtaining new network topologies of transistors is more useful than using the planar or standard FinFET devices. These extended work provoked for the new research, to make use of IG FinFET technology cost-effectively in VLSI design [14]. By using IG FinFET, a balance between power utilization and delay can be achieved when compared with that of planar transistors or standard FinFETs. Hence by the use of IG FinFETs, there is a reduction in the number of devices used to construct logic gates. From the single device, the probability of logical OR and logical AND operation are performed which emerges from the reduction in the count of transistors in logic gates. By the usage of single device operations, it may be implemented by providing low threshold voltage to the transistor. Regardless of the other transistor by the usage of only one device by conducting channels are formed if and only if one gate is active and when both the gates are active and when both the gates are active there is a higher inversion level [17]. Previously for the OR operation, low threshold voltage was applied but for AND operation high threshold voltage is applied. Therefore for AND gate operation both the gates must be an inactive state for constructing the conducting channel. In this study, it is proposed that IG FinFET explore the reduction of transistor count in the logic gates and their principle of individualistic feature double gate devices will be taken into account. Furthermore, from electrical simulations, the effect of power consumed from different topologies obtained from IG FinFET which is used to implement logic functions are studied. However, the delay in the logic circuit's critical path is determined by different input ranges, transistor series output characteristics and also by the stacks of such series in circuit [18]. In a decade for the construction of IC's more planar technology was used, However to reduce the length of the channel short channel consequence in sub threshold operation region is degraded. By reducing the short channel effects, reductions in the parameters of current, voltage, electric field and transistor length can also be increased by the application of MUGFETs. FinFETs are one of the most significant types of MUGFETs which provides more effective characteristics for the design of digital IC. In this chapter, characteristic and conduction of transistor and its electrical stimulation of IG, FinFET's are presented and after that fundamental working principle of independent gate transistors is given with a different configurable arrangement, threshold voltage and utilization of logic gates [19].

The FinFET based microprocessor designs are the most fundamental trends in the latest technologies such as

demand of semiconductor technology which is a group of basic building blocks such as ALU, registers, buffers, encoder and decoders and software trends that simulates or compiles the microprocessors [20]. Behind a considerable lot of these innovation patterns, the demand for semiconductors plays a basic job and profoundly impacts in their development, including the state of microchips. The most significant pattern in semiconductor innovation is the scaling of transistors, permitting of multiplying the quantity of accessible transistors on a chip for every year [21]. Notwithstanding this exponential development in devices, the scaling likewise accompanies an improvement in the presentation of every transistor device, empowering all the more dominant microchips in progressive ages. For sure, no other industry in history has seen the wonderful development that the microchip business has exhibited in the previous a very long while. FinFET has double Gate, so it has better control of channel from transistor gates, reduced short channel effects, with better Ion/Ioff and improves the sub-threshold slopes [22]. The power consumption in both dynamic mode and static mode are less as compared to traditional CMOS circuits. Here, the IC's design becomes most important aspect, due to its low cost, low area and high speed process activity. For two decades, low force/vitality configuration has been a significant structure limitation[23]. The trend in advanced battery lifetime, improve framework unwavering quality and decrease cooling costs has pushed for broad research in low force/vitality computerized structure. The static commotion edge of FinFET static random access memory (SRAM) cells working in the subthreshold region was explored utilizing an explanatory arrangement of 3-D Poisson's condition [24]. A diagnostic SNM model for subthreshold FinFET SRAM was shown and approved by 3-D innovation PC structure with blended mode reenactments. When contrasted with mass SRAM, the standard 6T FinFET cell indicated bigger READ SNM (RSNM), better fluctuation insusceptibility and lesser temperature affectability of cell [15]. Since, Moore's law-driven scaling of planar MOSFETs faces imposing difficulties in the nanometer system, FinFETs and Trigate FETs have risen as their replacements. Attributable to the nearness of numerous (two/three) entryways, FinFETs/Trigate FETs can tackle short-channel impacts (SCEs) better than traditional planar MOSFETs at profoundly scaled innovation hubs and in this manner empower proceeded with a transistor scaling. In this work, we inquire about on FinFETs from the bottommost gadget level to the highest design level [25-27]. We review various kinds of FinFETs, different conceivable FinFET asymmetries and their effect with novel rationale level and design level tradeoffs offered by FinFETs. We likewise show the investigation and enhancement that are accessible for portraying FinFET gadgets circuit models [16].

II. PROPOSED DESIGN OF 4-BIT NANO PROCESSOR DESIGN

Analysis of Power, area and delay for proposed 4-bit Nano-processor design: This research work mainly concentrates on the optimization of area, power and delay. The area is mainly depending on the number of transistors integrated to design the FinFET based processor using FinFET transistors and it can be expressed as $Area_{die} = \sum_{j=1}^{M} Size_j$, where $Area_{die}$ represents the silicon die area, M is the total number transistors integrated on single processor, $Size_j$ is the size of the each transistor. The total area of the FinFET based processor is designed by considering the various factors like total area die expected, wafer size and cost after fabrication for the market place. Afterward, the total area limitation or finalization of area for die, should then be met by the total sizes of incorporated each transistors. As the condition shows, one can either decrease the size of every transistor or essentially expel the necessary number of devices to fulfill this requirement. After the minimum size of the device is obtained using FinFET technology, rectifications of the violation for the area constraints are possible done and can be scaled down by transistor count. In this work, the area optimization is done by using "*fingering*" concept. Fingering is to upgrade the resistance of the gate poly terminal along the width of the transistor. Since, the gate poly is driven from one end and entryway poly is resistive, there might be motivation to have a rule that expresses the most extreme width of a solitary finger. But, the fingering requires more number of transistors but fingering concept will be the techniques to not only have area optimization, the active capacitance can also minimized because of the drain region is bounded with gate poly instead of the electric field.

*A.Technique to optimize the area by using Fingering Concep*t

- Keep a fixed size transistor so that the height remains constant, but then add more transistors in parallel to deliver more current to the load.
- In this case, join in clamped design mode with the source and drain terminal so that they act as taps in parallel. Through particular, when 2x and 4x drive force buffers are used, it will deliver 8 times more current than the normal 1x buffer by using 8 or even more fingers.

- Another benefit of fingering is that, the resistance significantly lowers. Let us just assume you have a resistance of R from as given, now all these resistances come in parallel when fingering is done, therefore, the resistance reduces by a factor of N, this is another notable advantage to fingering.

The second most parameter is power consumption or dissipation of the proposed processor chip which is measured as similar case of area discussed in above. This power is mainly depending on the cost-effective capacity cooling of more number of transistors i.e., for more volume processor designs. In the recent research, the energy in term of efficiency is optimized in different ways on the silicon chip budget. The power measurement in general is $P_{dissipationdie} = \sum(j=1..M)*Power_j$, where $P_{dissipationdie}$, is the power constraint on the chip design level, $Power_j$ is the power dissipated by the complete processor and M is the total number transistors used for the designing of the FinFET based processor.

In this research work, the 4-bit Nano-Processor is designed; with one of the constraint of this processor is analytic model of optimizing the power which is sum of the dynamic and static powers. The dynamic power is mainly due to switching activity of the transistor which is due to charging and discharging of the capacitor load at the output of the each and every transistor and it can be expressed as $Power_{dy} = C_l.V^2dd.F_{signal}$. The static power is because of spillage that has been consistently becoming in the course of the last few innovation ages. Sub-edge spillage, which has an exponential reliance with the limit voltage has expanded quickly with the scaling of edge voltage and commonly ruled the spillage flows. The limit voltage has nearly quit scaling to counter this sub-edge spillage; however, the scaling of other gadget parameters (e.g., oxide thickness) has caused an ascent in entryway spillage. In any case, there are a few instances of over-provisioning in the smaller scale design segments of current usage (e.g., the physical register document and guidance window passages). A FinFET based Nano-Multicore System (FinFET-NMS) is a class of multicores that by configuration arrangements of more handling center assets that can be kept dynamic for the objective of Thermal Design Power (TDP). The key differentiation between an ordinary multicore and a FinFET-NMS originates from the characteristic objectives in their framework structures, separately. Authoritative multicore considers a preparing center as one of the most basic segments of the framework and thus targets full use of it. A FinFET-NMS considers power and warm attributes more basic than the handling centers. In this proposed wok, the design consists of transistor with two controlling gates which is investigated as a circuit component and is utilized for the execution of various combinational basic components like gate, ALU, Multiplexers, Multipliers, CSA and encoder and decoders systems with utilizing these elements. The 4-bit Nano-Processor has been designed which depends on FinFET technology and is designed from Schematic level to layout using GDS-II level. The verification is done through physical design to validate the power, delay and area. With separately gates connected, series/parallel exhibit could be performed utilizing a solitary device. Various topologies got from the different gates activity were tried through electrical reenactments and the outcomes exhibit the current exchange off between these two parameters. Additionally, a diagnostic defer articulation was inferred for logic systems which use IG FinFETs, determining scientific articulations for the effect of diminishing varieties of arrangement of transistors in logic gates. The investigative model for IG-FINFET devices was tried in coherent information way and contrasted with SPICE reproduction results, demonstrating its utility for the planning examination of computerized circuit. In this work, mainly discussed about design of the ALU which includes all basic gates and arithmetic operation like multiplier, Carry Save Adder (CSA), MUX, 4-bit SRAM, Gilbert multiplier and buffers, through which the performance effects on the Nano-Processor is analyzed as shown in Fig.1. The complete processor design could be achieved and given in the following:

- The increase in source to drain current along with the simulation of electrical environment has been set-up and it is capable of controlling the nature of FinFET devices with gate controlling or coupling capacity.
- All transient electrical signals of different modules (discussed in the previous chapters) has been build using FinFET transistors and measured their performance metrics like delay and power dissipation.
- In order to measure the different equations of delay, transitions of the different modules based on FinFET logic structures, have been designed and compared with the existing work.

The FinFET device is a symmetrical transistor having same gate function as CMOS gate function i.e $G_1 = G_2 = G_{FinFET}$ and their oxide thicknesses are same i.e., $t_{ox1} = t_{ox2} = t_{FinFET\_ox}$. The gate and oxide thickness functions the control of the current flowing between source and drain which is very easy and can obtain the maximum current gain and voltage gain. The first part of design is 4 bit ALU using FINFET Technology. The CMOS Technology has the major issues of scaling of short channel effects like DIBL, sub thresholding and GIDL,

degradation of mobility and modulation of channel length. To address these issues with CMOS, the proposed design has been changed to mitigate technology formally called FINFET Technology. The main advantage of it are controlling of current since, it has two Gates, reduction of leakage current, reduction in delay of each transistor, minimum VT and also FinFET transistors operates at a low power levels. The main concentration of 4 bit ALU design is to optimize the power delay, area, V_T and leakage currents.

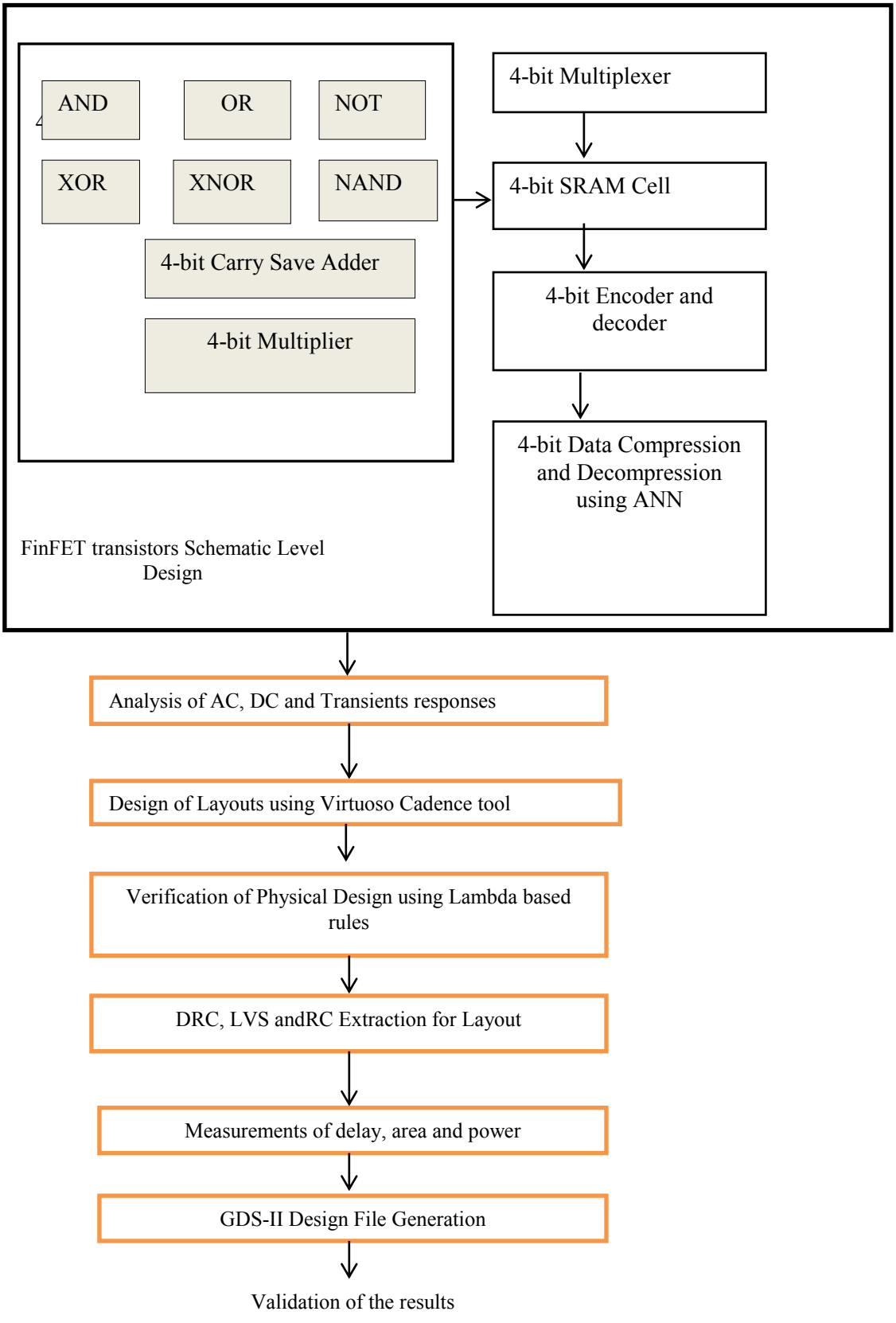

Fig.1 Proposed 4-bit Nano-Processor design using 32nm FinFET technology

The ALU consists of complex multiplier, comparator, substractor, carry save adder (CSA) which are the arithmetic operation and the seven logical gates are designed by 32 by using 32nm FinFET Technology for 4 bit as shown in Fig.2. The designed 4 bit ALU and its basic building block are used in the Nano processor. The 11 input multiplexer is designed to select one of the ALU outputs and given its input to MUX to get the desired output as shown in Fig.7.2. The first part of design is 4 bit ALU using FINFET Technology. The CMOS Technology has the major issues of scaling of short channel effects like DIBL, sub thresholding and GIDL, degradation of mobility and modulation of channel length. To address these issues with CMOS, the proposed design has been changed to mitigate technology formally called FINFET Technology. The main advantage of it are controlling of current since, it has two Gates, reduction of leakage current, reduction in delay of each transistor, minimum VT and also FinFET transistors operates at a low power levels. The main concentration of 4 bit ALU design is to optimize the power delay, area, V_T and leakage currents. The ALU consists of complex multiplier, comparator, substractor, carry save adder (CSA) which are the arithmetic operation and the seven logical gates are designed by 32 by using 32nm FinFET Technology for 4 bit as shown in Fig.2. The designed 4 bit ALU and its basic building block are used in the Nano processor. The 11 input multiplexer is designed to select one of the ALU outputs and given its input to MUX to get the desired output as shown in Fig.7.2.

III. RESULTS AND DISCUSSION

To meet power requirements, proposed Nano-processor must consolidate novel strategies for decrease in leakage current (LC), power decrease (PD), area optimization (AO) procedures. This work showed two explicit employments of LC, PR and AO contemplations utilizing scientific models in Nanoprocessor plan. In the first place, this work broadened the past work talked about in presentation and joined LC, PR and AO for unequivocally displaying power limitations in different Nano-Processors structures. This work found that with the expanding power imperative, demonstrated utilizing various degrees of LC, PR and AO, the uneven multicore moved towards the dynamic multicore. All structures of 4-bit Nano-processor cells of CMOS and FinFET were verified, validated and analyzed in term of simulation waveforms in Cadence Virtuoso tool to have metric investigations like different delays, normalized power consumption/dissipation, power-delay-product (PDP), energy and delay product (EDP). In light of these, the 4-bit FinFET-based Nano-processor is demonstrated to be the most minimal and ideal tradeoff in every single metric execution contrasted with the CMOS-based existing processor as shown in Fig.3. This work mainly concentrated on the design of 4bit Nano-Processor and characterization of FinFET standard cell library of 32nm in Cadence Virtuoso bundle. The first part of this research work is to design of 4bit ALU, it includes all gates, multiplier, fast Carry Save Adder (CSA) and multiplexer. All individual logical and arithmetic modules are design from schematic level to generation of Graphic Data System (GDS-II) level through layout design, DRC and LVS; therefore, the 4-bit ALU can be fabricated as chip. The ALU is designed by using CMOS inverters and the designed ALU schematic is simulated through 32nm FinFET technological library and compared with CMOS technology which is simulated through 32nm CMOS library (without FinFET). The power consumption of AND, OR, XOR, NOT and NAND gates are 36.09nW, 64.970nW, 61.13nW, 33.31nW and 37.45nW respectively. The basic gates and universal gates, CSA, subtraction and MUX are integrated for 4-bit ALU design and its delay, power consumption and area are 0.104nsec, 314.4uW and 56.8usqm respectively.

This demonstrated that by utilizing FinFET innovation in 4-bit processor chip level circuitry, it will improve its characteristics parameters in terms of power, area and delay. In any case, the cell configuration likewise adds to how better the nano-processor performs, as examined with prior. The 4 bit FinFET based Nanoprocessor has a decreased propagation delay with normal energy dissipation, PDP along these lines giving FinFET innovation incredible points of interest in vitality effectiveness for 32 nm innovation. It was likewise confirmed that the 4-bit conventional pass-transistor logic (CPL) FinFET based nano processor performed very well with a decreased measure of PDP contrasted with other cell plans on account of its fast execution and full swing activity. The complete Nano-processor design which includes ALU, Multiplexer, encoder, decoder and ANN schematic in terms of analog transistors are shown in Fig.7.3. The results are validated through simulation of each and every sub components as shown in Fig.4.

The Fig.4 is ANN design, as it includes both compression, decompression and their input and output ports. From the result it is clear that, the delay and power simulations of the designed Nano-Processor were performed to prove that 32nm FinFET transistors is quite better to minimize the leakage currents and have the area optimization using Fingering concept. From the obtained results, it is observed that, there is reduction power of about 48%, reduction in delay is about 51% and 29% of
power reduction as compared to existing works.

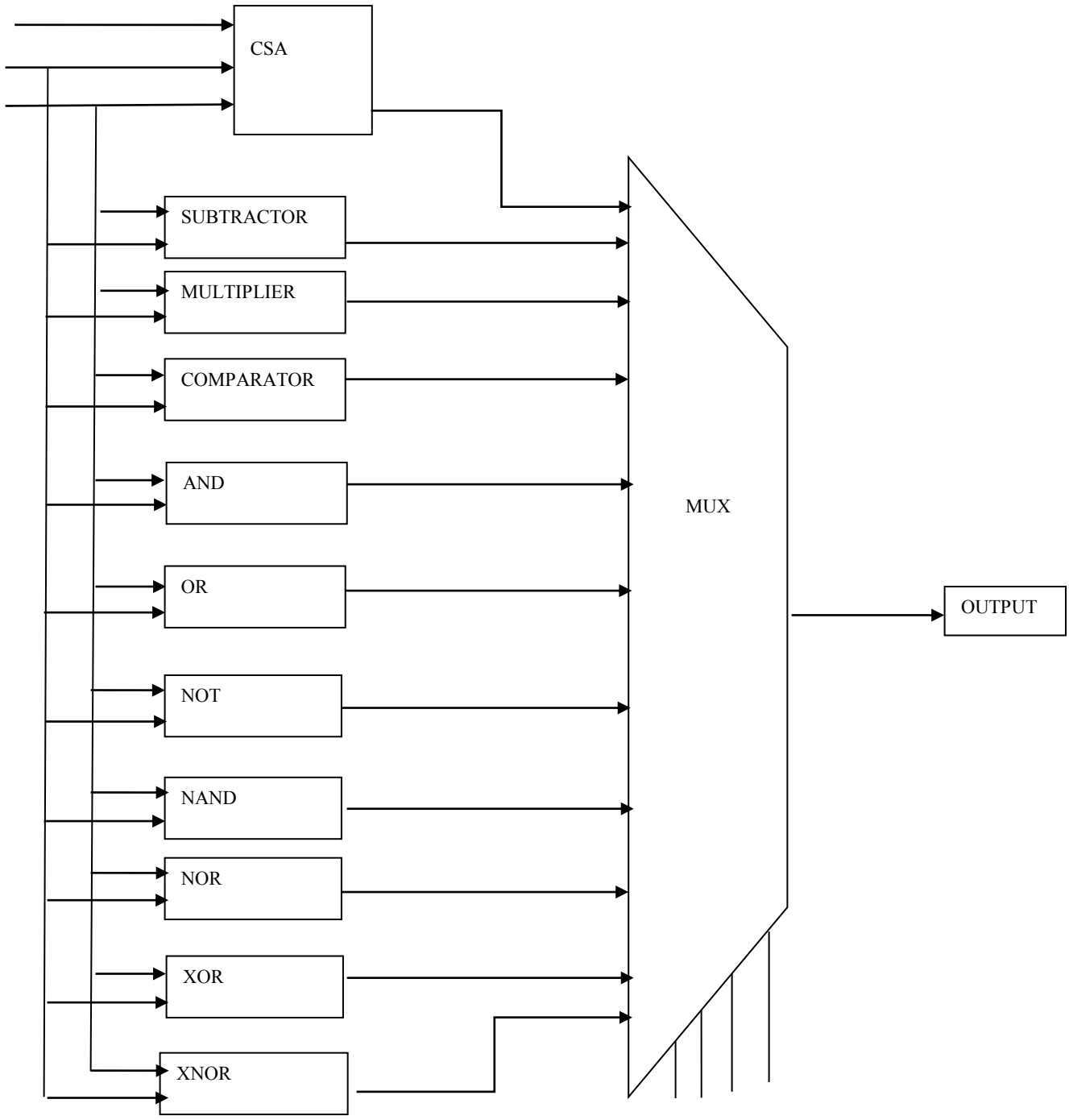

Fig.2 Architecture Of 11bit ALU with 11 Input MUX

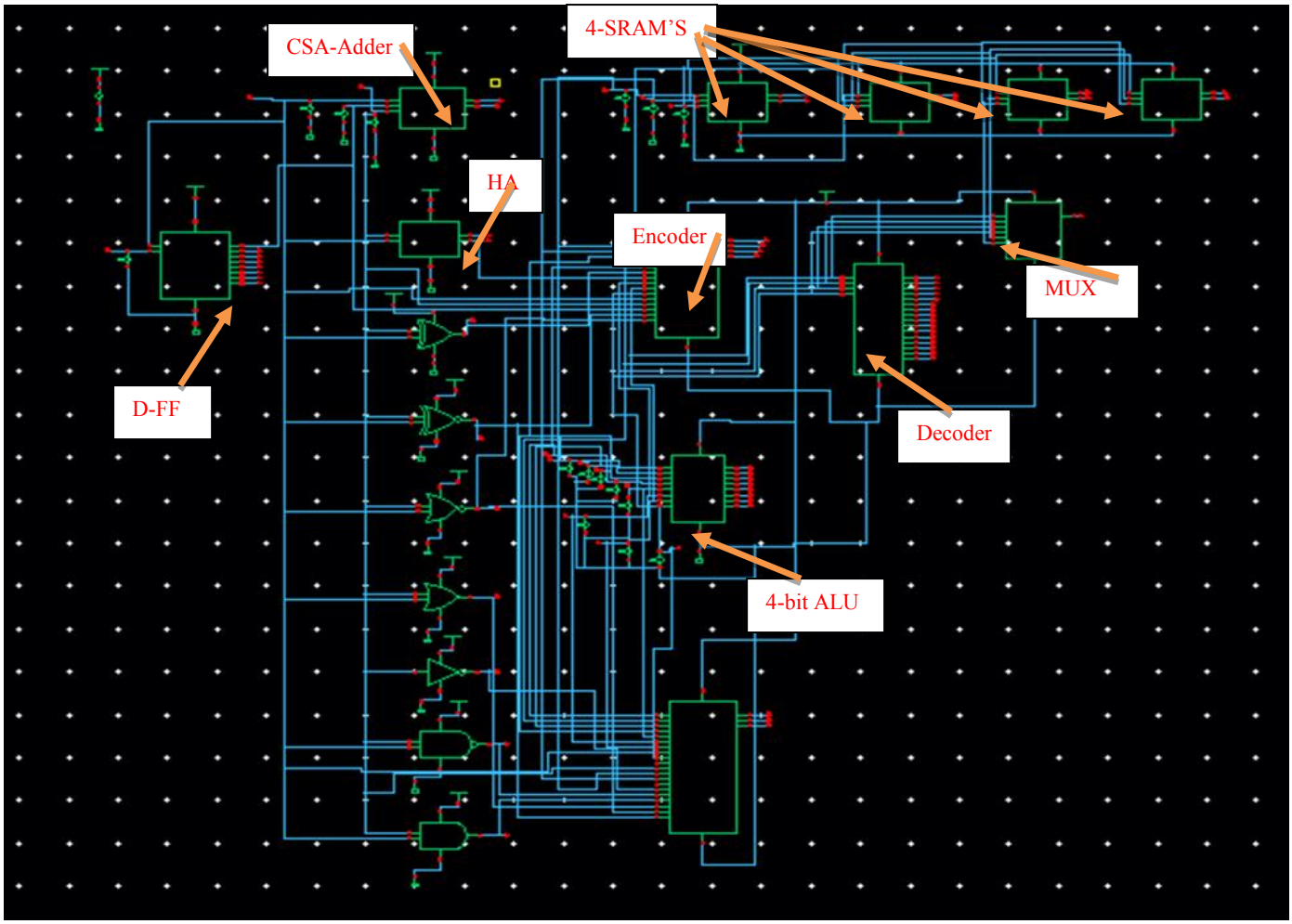

Fig.3 Overall proposed Nano-Processor design using FinFET 32nm technology and subcomponents.

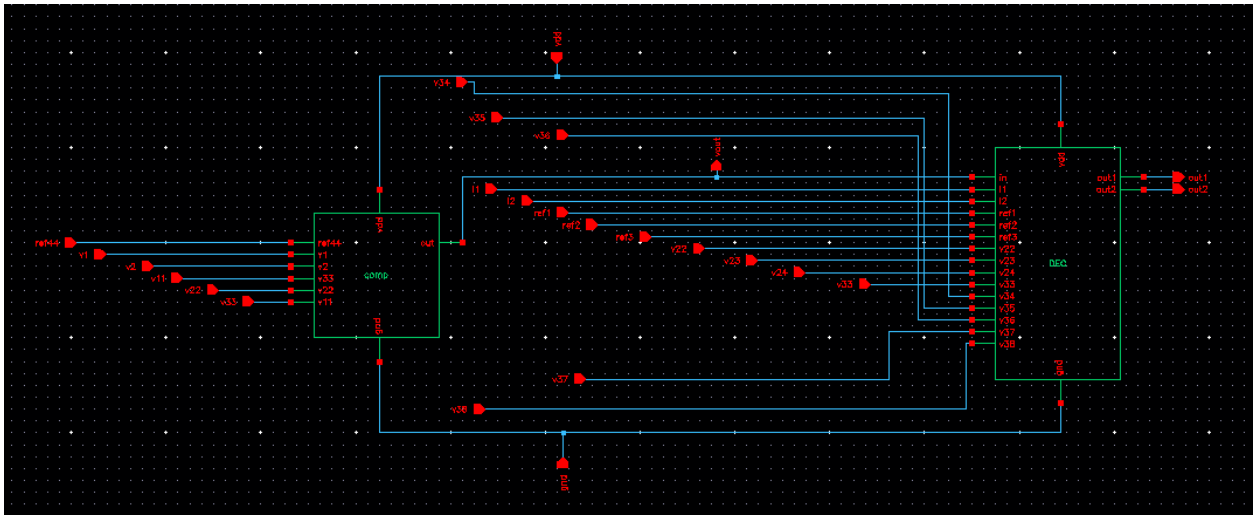

Fig.4 Top level schematic circuit of ANN

IV. CONCLUSION

In this work, the design having all basic operations with ALU, multipliers and using these basic elements, the 4-bit Nano-Processor is designed. This processor design, show the interested feature of FinFET devices for controlling of the current flowing between source and drain and controlling of the transistor operations to obtain better gain, low power, less delay and minimal area. Through dual gate operation, it is observed that, the threshold voltage (V_t) is minimum when compared to the case in the CMOS technology. The complex multipliers and other complex logical functions are simulated using Virtuoso back-end Cadence tool which include the 32nm FinFET technology. The simulated results using different topologies have shown that reduction in the number of transistors, low area and optimized power is obtained. Lastly, delay and power simulations of the designed Nano-Processor were performed to prove that 32nm FinFET transistors would be helpful to minimize the leakage currents and area optimization using Fingering concepts. From the obtained results, it is observed that, there is reduction power of about 48%, reduction in delay is about 51% and 29% of power reduction as compared to existing works.

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