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A Novel Conditioning Circuit for Floating-Gate ISFET Bio-Sensor

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Abstract: Floating-Gate-Ions-Sensitive-Field-Effect-Transistors (FG-ISFETs) are becoming the sensor's platform for various fields such as biomedical and chemical sensors. Despite many advantages like quick response, small size as well as wide measurement range, the efficiency of the output measurement is widely affected by temperature, This requires more safety in the measured results and the analysis's tools. This study describes a novel integrated circuit that improves the thermal stability of the output signal of the ion-sensitive field effect transistors (ISFETs). After that, we investigate the temperature dependency of the FG-ISFET using the mentioned macro model and we shows that the temperature coefficient is about of 6 mV/°C. Afterward, a new integrated interface circuit that can perform great temperature compensation was developed. This operation aims to enhance stability of readout circuit for FG-ISFET. The achieved result of the FG-ISFET under different simulations shows that the readout circuit has a good temperature compensation i.e. :2.4 10^{-9} mV/°C.

Keywords: FG-ISFET, Temperature dependence, conditioning circuit, TopSPICE, ADS.

I. INTRODUCTION

The Floating-Gate Ion-Sensitive Field-Effect Transistors (FG-ISFETs) since their introduction over decades ago, have become essential today due to their many applications in very varied fields[1-4]. They are widely used in biology, biochemistry, medicine, security, agriculture and the environment [5-8]. The detection of a chemical species as well as the evaluation of its concentration in all fields related to chemistry and biochemistry can be modelled using chemical instruments more commonly called micro-sensors, which have the advantage of being compatible with microelectronic technologies [9, 10]. Recently, many works have used the FET sensors to track and investigate the covid-19 virus for faster diagnostics and environmental monitoring[11-13]. An article create by Jingui[14]shows that both of laboratory and epidemiological studies prove that ambient temperature affect the survival and transmission of Corona viruses. However, the FET sensor has experienced inherent difficulties including their function due the instability of the environments which can modify their properties and therefore their characteristics[15]. Temperature is an important parameter, particularly for sensors made up of semiconductors. It is well known that variations in temperature affect the performance of the sensors [16-18]. The influence of temperature can also be specified more generally by the error on the sensitivity[18, 19]. The interference of temperature is frequently observed in inaccurate measurements[19, 20]. To solve this problem and improve the stability of FG-ISFET, some work has been done in the past decades, including simulations of its characteristics as a function of temperature according to a theoretical model. The result shows that the temperature dependency of FG-ISFET is complicated in nature while the user uses them under variable environmental conditions. Moreover, the FG-ISFET's temperature dependency tends to exhibit a random behaviour [21, 22]. The straight line based temperature compensation limits its scope when dealing with the actual nonlinear temperature characteristic of FG-ISFET micro-sensor for different values. Besides, the conditional-circuit eventually introduces an additional temperature coefficient on the measured data [23, 24]. Therefore, the ease of combining the efficiency of the compensation technique and the temperature compensation circuit became the key design for the integrated circuit. Respectively, it is challenging for FG-ISFET sensor to operate in an instable environment where the required task is to track the variation of the

pH concentration for different values of temperature [25]. However, conventional devices used in the signal processing of FG-ISFETs, especially basic current-voltage conversion circuits, cannot achieve the optimal performances because they are sensitive to the variation of the temperature and light. In this work, the first challenge is to validate the FG-ISFET macro model with the experimental data here we used for the first time the TopSPICE tool to model and validate the FG-ISFET macro-model. After that, we intensively investigate the temperature effect on the FG-ISFET and gives at the end a robust and reliable solution to reduce the interference of the temperature.

In this work, we initially compare and validate the FG-ISFET macro-model with experimental data, subsequently we investigate the temperature dependency of the validated FG-ISFET. After that, a novel read-out circuit is presented and a conclusion is drawn in the final section.

II. COMPACT MODEL

The considered FG-ISFET macro-model that captures the current-voltage (I-V) characteristics is based on the model developed under HSPICE [26]. The FG-ISFET macro-model as referred in [26] has two gates connected to the floating gate (FG), the first one referred as the sensing-gate (SG), the second is called the control-gate (CG). As shown in figure 1, the gate potentials are the V_{CG} for the control Gate and φ_0 for the sensing gate (SG).

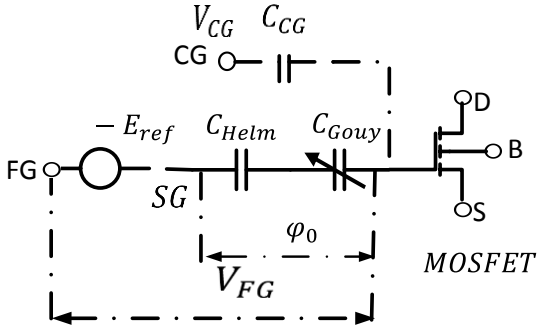


Figure1: Floating-Gate ISFET macro-model

The equation (1) describe the device operation by considering the floating gate potential (V_{FG}):

$$V_{FG} = \frac{C_{CG}V_{CG}+C_{SG}\varphi_0}{C_{TOT}} + \frac{C_{GS}}{C_{TOT}}V_S + \frac{C_{DS}}{C_{TOT}}V_D + \frac{Q}{C_{TOT}} \quad (1)$$

And by considering the floating gate potential V_{FG} and I_{DS} current in the saturation regime, we get:

$$I_{ds} = U_n \frac{C_{ox}W}{2L}(V_{FG} - V_T)^2 \quad (2)$$

where V_T is the threshold voltage of the MOS transistor, U_n refers to the carrier mobility, C_{ox} grid surface capacity, L,W are the length and width of the channel. In the simulation the net-charge Q at the floating gate is zero. Deviation from the assumptions are constant shift in the V_T. Also, experimentally found that The capacitances C_{GS} and C_{GD} are insignificant interfering on the sensor behaviour and can be neglected[26]. These can be simply combined in the presented compact macro-model in SPICE. The sensing terminals of the FG-ISFET are composed of the floating gate, sensing membrane, reference electrode and electrolyte is modelled with behavioural source voltage in SPICE. Figure 1 illustrate the synoptic presentation of the FG-ISFET macro model. Compared to other capacitances, the electrolyte capacitance is much larger and the coupling of sensing gate and the reference electrode are expressed as follows:

$$\varphi_0 = V_{REF} + V_{cell}^0 + V_{pH} \quad (3)$$

Where V_{REF} stands for the reference voltage, V_{cell}^0 refers to the interfacial constant potential associate to electro-chemical cell and the V_{pH} describes the potential that is proportional to the variation the concentration in the electrolyte. The device functioning and the voltage sources in series in the electrochemical cell are explained using this approach. Thus, it is clear from the equation (3) that V_{pH} and the surface potential φ_0 are interlinked. Moreover, we must-note that the macro-model assumes that the V_{REF} is equal to the solution bulk voltage. Also, the V_{REF} may simply include junction potential corrections.

1. MODEL DEFINITION:

A TopSPICE sub-circuit is used to solve the model. Standard SPICE circuit components are used to emulate the FG and CG nodes, which are capacitors coupled to MOSFET. Figure 1 illustrates a block schematic of the macro model. The sub-circuit has six input nodes: the reference electrode (FG), the control gate (CG), the source (S), the drain (D) and the bulk (B). To control the variation of the pH we adjust the values of V_{FG} which is directly proportional to the surface potential φ_0[26]. Since the sensor is controlled from the floating gate via the oxide, this macro-model present in figure 1 is sufficient for our sensor structure, this model exhibits the electrochemical activity, and can be used to design pH sensors or FG-ISFET based microsystems.

2. FABRICATION AND TESTING

The sensor used in this work was fabricated at the Research Institute of Micro-devices NAS of Ukraine. As shown in figure 2, the sensors ship contains two identical ISFET's, these sensors were micro-machined on P-type wafer and the dimension in about of 3 x 10 mm. The sensor chip was connected to the aluminium conductors and mounted to a Sital (fused silica) support.

Besides, as shown in figure 2, the sensor terminals were encapsulated with epoxy-resin [27] [45].

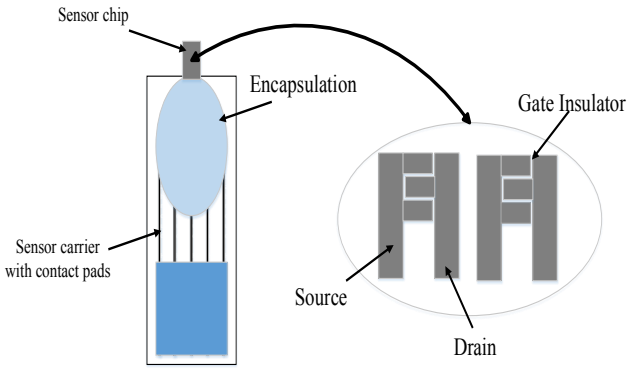


Figure2. Sensor chip design.

To measure drain-source current (I_{ds}) as a function of gate-source voltage V_{ds} of the ISFET, the gate-source voltage V_{gs} was fixed at 1 V and the source and the substrate are grounded as shown in figure 3. In order to estimate the sensitivity of the sensor we used three buffer concentration goes from pH =3 to pH =7. The temperature impacts on the FG-ISFET responses were studied to explore the pH sensor's reliability and stability. Temperature can alter the characteristics of a sensor, the pH of the electrolyte, the voltage of a reference electrode, and the measuring system. The temperature within the room was kept constant during the latter modifications. A heat-regulating circuit with a temperature sensor and a heating system was utilized to keep the electrolyte, electrode, and FG-ISFET at a steady temperature. figure 3 (a) illustrate the sensor that we used for the extraction of the experimental data, figure 3(b) indicates the FG-ISFET macro-model, the V_{FG} which is directly proportional to the surface potential φ_0 and reference electrode and the V_{CG} is the control gate voltage which is proportional to the capacitance C_{CG}.

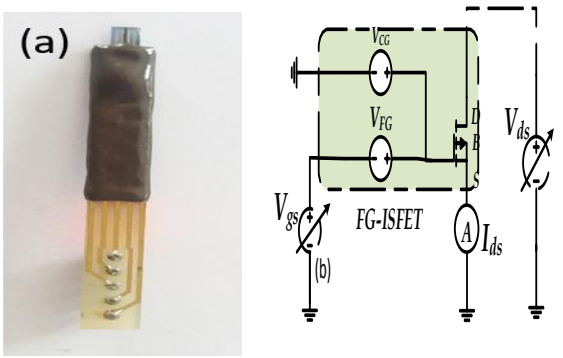


Figure 3. (**a**) ISFET top view, (**b**) TopSPICE circuit simulation using the FG-ISFET macro-model.

In the experiment, for V_{gs} we used a simple DC generator; for the variation of the V_{ds} *we used* GW Instek SPS-606; to measure the I_{ds} we used the Keithley-2400 Source-Meter. Figure 4, shows the extracted results from the FG-ISFET macro-model and the recorded data from the experiment:

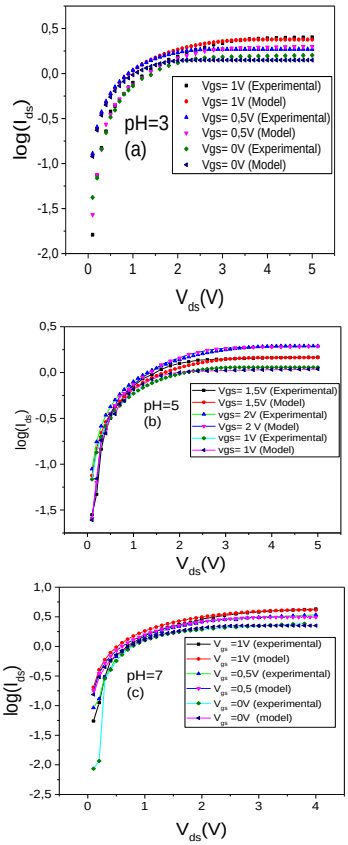


Figure 4. Macro-Model versus experimental data.

By analyzing the figure 4, we notice that there is a good match between the FG-ISFET model and the experimental data. The extracted data from figure 4 are plotted as a function of pH in figure 5. The estimated sensitivity of FG-ISFET macro-model is in order of $s_m = 44\ mV/pH$ and for the experiment we found the sensitivity is about of $s_{exp} \approx 41\ mV/pH$. We notice from figure 6 that the macro-model and the experimental data has approximately the same slope. Indeed, we can conclude that the FG-ISFET macro-model can predict efficiently the values of pH. In this section, using for the first time the software TopSPICE we succeeded to compare the FG-ISFET with the experimental data. Most of the researchers have been used the HSPICE or LTSPICE [13, 28-31] simulators to model the FG-ISFET sensor in this work we illustrate that it is possible to use the TopSPICE as an alternative to model the FG-ISFET sensor. TopSpice is a PC-based mixed-mode analog/digital/behavioral circuit simulator. From schematic capture to graphical waveform analysis, it delivers the most powerful SPICE simulator in its price range, scalability, and an easy-to-use integrated design environment[32].

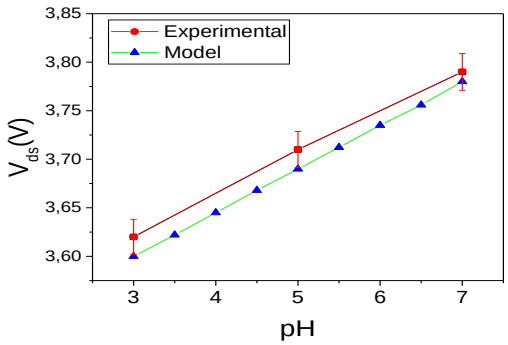


Figure 5. V_T as a function of the pH.

Table 1 reports the list of the technical parameters that were employed in the ISFET macro model:

Table 1. SPICE parameter of the Floating Gate ISFET

Parameter	values
V_{to} (Threshold voltage (v))	-2.2
T_{ox}(oxide thickness (m))	200e-9
U_{exp}(Surface Mobility, (cm^2/(Vs)	7.64E-2
N_{sub} (silanolsurface site density)	3.27E15
N_{nit} (amine surface site density)	2 E15
XJ (Metallurgical Junction Depth(m))	6.01E-9
CJ (Zero-bias Bulk Junction Cap (F/m^2)	4.44E-4
C_{JSW}(Zero-bias Bulk Junction Sidewall Cap(F/m))	5.15E-10
Phi(Surface Potential (V)	0.5

III. The Dependence of the Threshold Voltage as a Function of the Temperature:

The temperature behaviour of Floating-Gate-ISFET (FG-ISFET) is more complex than the MOS transistor. The temperature effect extends not only to a semiconductor part of FG-ISFET, but also the electrochemical part including the reference electrode [33]. The variation of the threshold voltage as a function of temperature in FG-ISFET structure is given by equation 4:

$$\frac{dV_{T_{FG-ISFET}}}{dT} = \frac{dV_{T_{MOS}}(T)}{dT} + \frac{dE_{Ref}(T)}{dT} + \frac{d\Delta\varphi^{lj}(T)}{dT} - \frac{d\varphi_0(T)}{dT} + \frac{dX^{sol}(T)}{dT} \quad (4)$$

Where,$V_{TG_{ISFET}}$ is the FG-ISFET threshold voltage,$V_{T_{MOS}}$ is the threshold voltage of MOS Transistor, E_{Ref} is the reference electrode voltage, X^{Sol}refers to surface dipole potential, $\Delta\varphi^{lj}$ potential drop, φ_0 surface potential. As shown in equation (4) FG-ISFET is sensitive to temperature variation as the semiconductor and electrochemical parameter are temperature-dependent, which leads to distort the output signal. The threshold voltage $V_{T_{FG-ISFET}}$ is proportional to the variation of temperature and the concentration of the solution. As consequence, the variation of the Temperature effect transistor parameters such as interface charges at electrolyte/insulator interface, reference electrode potential and surface dipole potential of the solution. Also, Referring to [33] the electrolyte/insulator surface potential is directly proportional to the variation of the temperature. In the following section we investigate each parameter influenced by the variation of the temperature.

1. The Effect of Temperature on the Characteristics of MOSFET:

According to the MOSFET theory's and using the third level of PSPICE model, the temperature effects on the MOS Transistor is shown in two phenomena the first the degradation of mobility μ_{eff} of the channel and the threshold voltage $V_{T_{MOS}}$. The following expression (5) illustrate the dependency of the threshold voltage on the temperature:

$$V_{T_{MOS}}(T) = V_{FB}(T) + \emptyset(T) + \gamma\sqrt{\emptyset(T)} \quad (5)$$

Where V_{FB} refers to the flat band voltage, γ is the effect factor, $\emptyset(T)$ refers to inversion potential on the surface and it can be expressed as follows:

$$\emptyset(T) = \emptyset(T)\frac{T}{T_{nom}} - 3\frac{KT}{q} log\left(\frac{T}{T_{nom}}\right) - E_g(T_{nom})\frac{T}{T_{nom}} + E_g(T) \quad (6)$$

$$\text{Where } E_g(T) = 1.16 - 0.000702\frac{T^2}{T+1108} \quad (7)$$

Where T is the absolute temperature, K Boltzmann constant. The mobility of the carriers μ_{eff} in the inverted layer is defined by:

$$\mu_{eff}(T) = \frac{\mu_S(T)}{1+\frac{V_{DE}}{V_C(T)}} \quad (8)$$

$$\text{Where } V_C(T) = V_{max}\frac{L}{\mu_S(T)} \quad (9)$$

$$\mu_s(T) = \frac{\mu_0}{1+\theta(V_{gs}-V_{TH})\frac{V_{DE}}{V_C}}\left(\frac{T}{T_{nom}}\right)^{-1.5} \quad (10)$$

Where V_{DE} = max (VDS, VDSAT), θ is the mobility modulation factor which we assume to be independent

of the temperature, V_{max} is the speed limit carriers in the channel and L the length of the channel.

2. REFERENCE ELECTRODE POTENTIAL:

In FG-ISFET the reference electrode serves to supply a constant voltage to the electrolyte. The dependency of the reference electrode as a function of the temperature is as follows:

$$E_{ref}(T) = E_{abs}\left(\frac{H^+}{H_2}\right) + E_{ref}\left(\frac{A_g}{A_gCl}\right) + \left(\frac{dE_{ref}}{dT}\right) \times (T - 298.16) \quad (11)$$

where, $E_{abs}\left(\frac{H^+}{H_2}\right)$ refers to hydrogen (H+) potential with a standard values in order of 4.7 V and $E_{ref}\left(\frac{A_g}{A_gCl}\right)$is the relative potential with a standard value about of 205 mV [34-36]. By simplifying the equation (11) we found:

$$E_{ref}(T) = 4.905 + 1.4 \times 10^{-4} \times (T - 298.16) \quad (12)$$

3. SIMULATION RESULTS:

By examining the figure 6 we notice that the drain I_{ds} of the FG-ISFET differs with the temperature variation. The increase of the temperature causes the deterioration of the drain current. This deterioration is explained by the presence of two phenomena the first one is modelled by the degradation of the mobility µ and the second is the variation of the *threshold voltage* V_T, as a consequence the drain-source voltage V_{gs} varies considerably when the temperature varies.

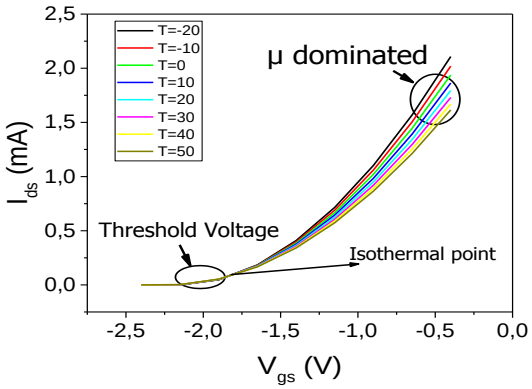


Figure 6. $I_{ds} = f(V_{gs})$ as a function of temperature from -20°C to 50°C.

Figure (6) shows the variation of the drain-source current for different values of temperature. The interference of the temperature is well observed in the saturation regime. The drain current is widely affected by the variation of the temperature and we notice that when Vgs goes from -1 V to -0.5V the current varies considerably, this variation is caused by the degradation of the mobility µ [11] [14]. To investigate more the temperature interference on the output signal of FG-ISFET, figure 7 shows the variation of the surface potential of the micro-sensor as a function of pH for different values of temperature. The instability of the drain-current provokes the degradation of sensitivity for wide range of pH when the temperature goes from -20 to 50 °C.

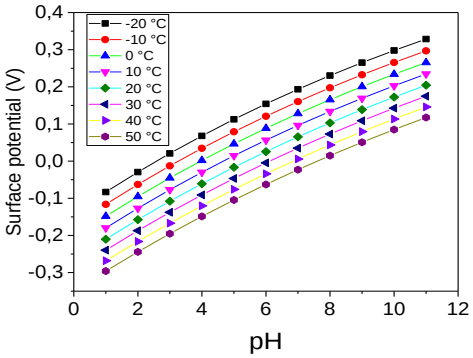


Figure 7. the surface potential as a function of pH for different values of pH

To prove more the instability of the sensor when temperature varies, figure 8 shows the sensitivity of the sensor when pH ∈ [1, 5, 10] when temperature goes from -20°V to 50 °C. we clearly notice by inspecting the plots of figure 8 that for each value of temperature the output signal varies, the temperature coefficient found in figure is about of 6 mV/°C, over 15 % is affected by the temperature.

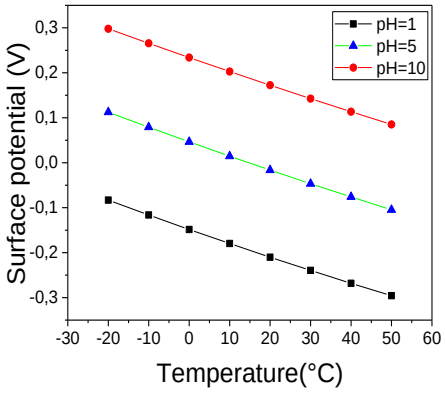


Figure 8. Sensitivity as a function of temperature.

As shown in this section the strong dependence between the output signal of the FG-ISFET and temperature, it is necessary to find a robust solution to compensate the temperature effects. In The next section, a new conditioning architecture that is capable to reduce the temperature effects on the output signal is proposed.

IV. THE OPTIMIZED SOURCE FOLLOWER ISFET READOUT CIRCUIT:

The validated model under TopSPICE in section 2 is exported as a netlist to the emulator Advanced Design System (ADS). We choose to work with ADS because

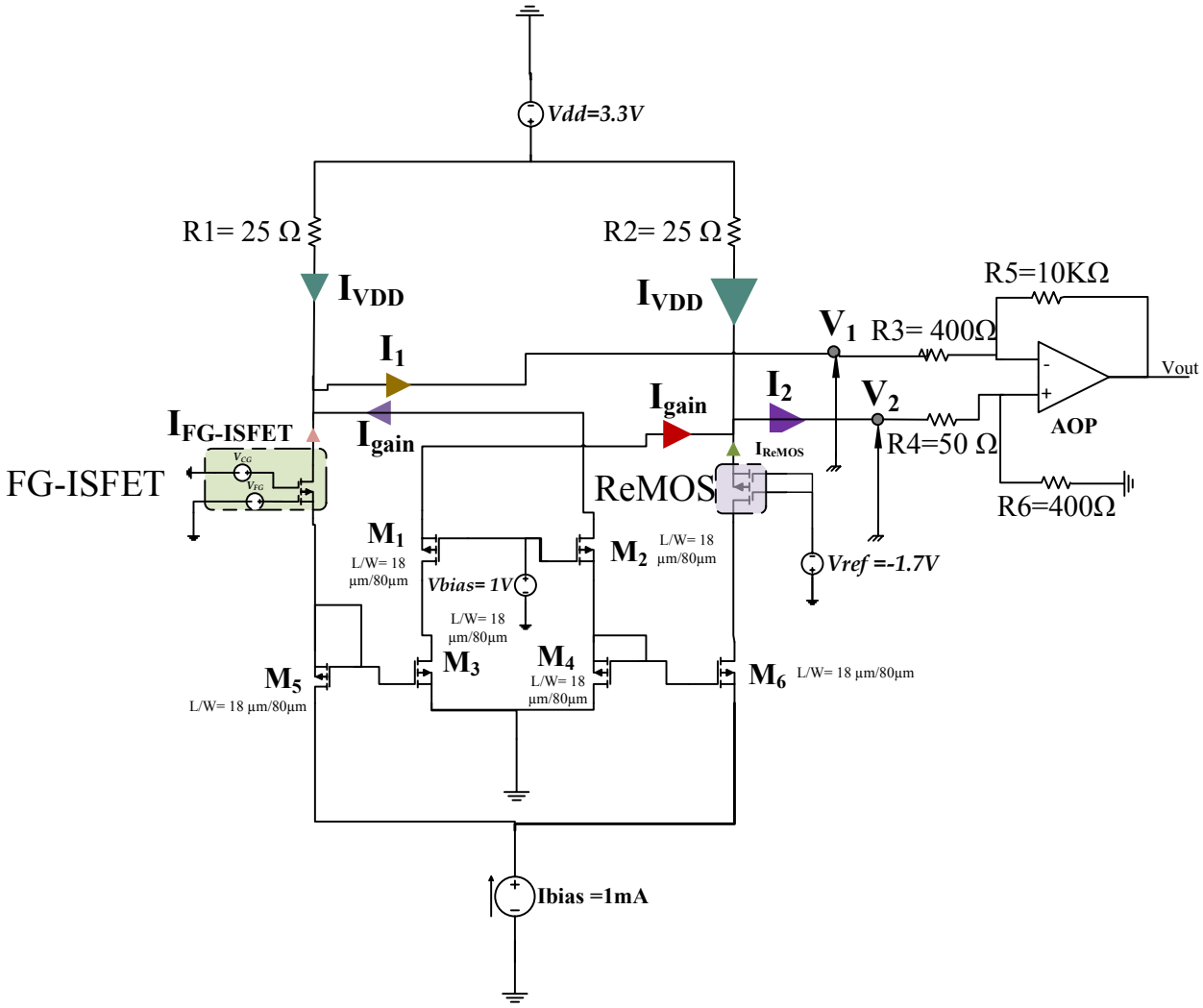


Figure 9. The proposed circuit for temperature compensation in ADS

is ranked as one of the best simulator tools for signal processing[37]. The ADS circuits emulator is a sophisticated frequency and time-domain simulator of linear and nonlinear circuits [44]. As proven in section 3 the FG-ISFET has a strong temperature dependency, to overcome this issue we propose in figure 9 a new conditioning circuit in order to reduce the interference of the temperature. The presented circuit in figure 9 is based on the FG-ISFET/ ReMOS, this topology has the ability to insure the multiple FG-ISFET detection because the refence electrode is grounded with mean that we can use one single electrode for many ISFET's. Also, the presented circuit in figure 9 is recommended for FG-ISFETs with unknown technical specification because it has a large range of operations. The circuit in figure 9 has been designed using ADS.

In this work we choose to work under staturation regime beacause as it proven in the last section in the temperature interfere considerably on the output signal espacialy when V_{gs} operate in the saturation regime. Equations 13 and 14, shows the exprression of the currents I_1 and I_2 (present in figure 9):

$$I_1 = I_{FG-ISFET} + I_{gain} + I_{VDD} \quad (13)$$

$$I_2 = I_{ReFET} + I_{gain} + I_{VDD} \quad (14)$$

Where
$\boldsymbol{I_{FG-ISFET}}$ *refers to Ids of the FG ISFET, and* $\boldsymbol{I_{gain}}$ refers to the current delivered from the transistor M_1 and M_2 which is directly proportional to the $\boldsymbol{V_{bias}}$variation, $\boldsymbol{I_{ReFET}}$ refers to the reference MOSFET and $\boldsymbol{I_{VDD}}$ stands for current from the V_{dd} generator. Hence, the expression of the amplifier inputs V_1 and V_2 are as follows:

$$V_1 = I_1 R_3 + I_2 R_4 \quad (15)$$

$$V_2 = I_2 (R_4 + R_2) \quad (16)$$

For $V^+ = V^-$ the expression of the output signal V_{out} is as follows:

$$V_{out} = \frac{R_6}{R_4}(V_1 - V_2) \quad (17)$$

After replacing V_1 and V_2 by their expressions, the output voltage became:

$$V_{out} = \frac{R_6}{R_4}(I_1R_3 + I_2R_4 - I_2(R_4 + R_6)) (18)$$

$$V_{out} = \frac{R_6}{R_4}(I_1R_3 - I_2R_6) (19)$$

For $R_3 = R_6 = R$ *and* since we work under saturation regime the expression of V_{out} became as follows:

$$V_{out} = \frac{R_6}{R_4}\left(RU_n\frac{C_{ox}W}{2L}\left(\left(V_{FG} - V_{T_{FG-ISFET}}\right)^2 - (V_{FG} - V_{ReFET})^2\right)\right) \quad (20)$$

$$V_{out} = \frac{R_6}{R_4}\left(RU_n\frac{C_{ox}W}{2L}(V_{FG}{}^2 - 2V_{gs}V_{T_{FG-ISFET}} + V_{T_{FG-ISFET}}{}^2 - V_{FG}{}^2 - 2V_{FG}V_{T_{ReMOS}} + V_{ReFET}{}^2\right) (21)$$

$$V_{out} = \frac{R_6}{R_4}\left(RU_n\frac{C_{ox}W}{2L}(-2V_{FG}(V_{T_{FG-ISFET}} - V_{T_{ReMOS}}) + V_{T_{FG-ISFET}}{}^2 - V_{ReFET}{}^2)\right) \quad (22)$$

Where $V_{T_{ReFET}}$ *and* $V_{T_{FG-ISFET}}$ refers respectively to the ReMOS and FG-ISFET threshold Voltage. As shown in (22) V_{out} is proportional to the threshold voltage of FG-ISFET which is also proportional to the variation of the pH, as consequence, the pH variation is directly proportional to temperature. The equation (23) show the dependence between the threshold voltage of the FG-ISFET and the temperature:

$$V_{T_{FG-ISFET}}(T)_{T=T1} = V_{T_{FG-ISFET}}(T_0) + KVT_{(pH)}(T_1 - T_0) + 2.303U_t\alpha(pH_{pzc} - pH) \quad (23)$$

Where $V_T(T)_{T=T1}$ refers to the threshold voltage as a function of temperature, $V_{T_{FG-ISFET}}(T_0)$ stands for the threshold voltage at ambient temperature, K_{VT}*is* the temperature-coefficient of the threshold voltage, which is usually varies from -0.5 mV/°C and -3 mV/°C. pH_{pzc} refers to pH at point zero charge, α is a correction-coefficient that ranging from 0 to 1. In addition, the dependence between the threshold voltage of the ReMOS and the temperature is as follows:

$$V_{T_{ReFET}}(T)_{T=T1} = V_{T_{ReFET}}(T_0) + K_{VT}(T_1 - T_0) \quad (24)$$

Besides, the temperature dependency of resistances R, R_4 *and* R_6 can be modeled as follows:

$$R = R(T = T_0)((1 + \lambda(T_1 - T_0)) (25)$$

Where $R(T = T_0)$ is resistance value at $T = T_0$, λ refers to the temperature-coefficient of the resistance material. As a consequence, the expression (23) became as follows:

$$V_{out} = \frac{R_6}{R_4}\left(RU_n\frac{C_{ox}W}{L}(-2V_{FG}(V_{T_{(pH7)}}(T_0) + KVT_{(pH)}(T_1 - T_0) + 2.303U_t\alpha(pH_{pzc} - pH) - V_{T_M}(T_0) - K_{VT}(T_1 - T_0)) + \left(V_{T_{(pH7)}}(T_0) + KVT_{(pH)}(T_1 - T_0) + 2.303U_t\alpha(pH_{pzc} - pH)\right)^2 - \left(V_{T_{(pH7)}}(T_0) + KVT_{(pH)}(T_1 - T_0)\right)^2\right) (26)$$

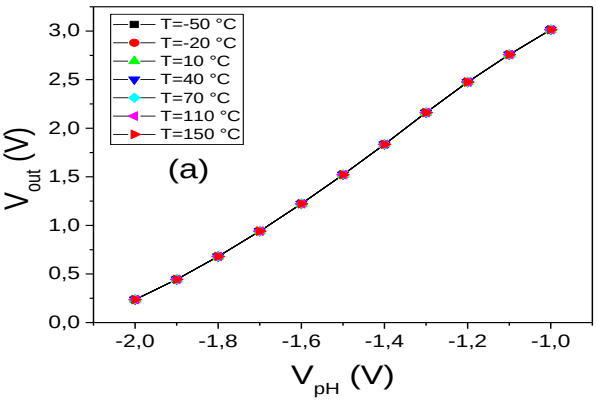
After arrangement, the output signal as a function of temperature become as follows:

$$V_{out}(T_1) = \frac{R_{6(T_1)}}{R_4(T_1)}\left(R(T_1)U_n\frac{C_{ox}W}{2L}(-2V_{gs}2.303U_t\alpha(pH_{pzc} - pH)) + \left(2.303U_t\alpha(pH_{pzc} - pH)\right)^2\right) (27)$$

Since we used FGISFET/ReMOS topology we assumed that the two devices has the same threshold voltage and the K_{VT}. The (27) demonstrates the efficacy of the suggested circuit for temperature reduction.

1. Results and Discussion

The presented circuit in figure 9 was simulated under severe temperature range goes from -50 °C to +150 °C. Figure 10 shows the evolution of the output voltage as a function of the V_{pH} voltage for different values of temperature:



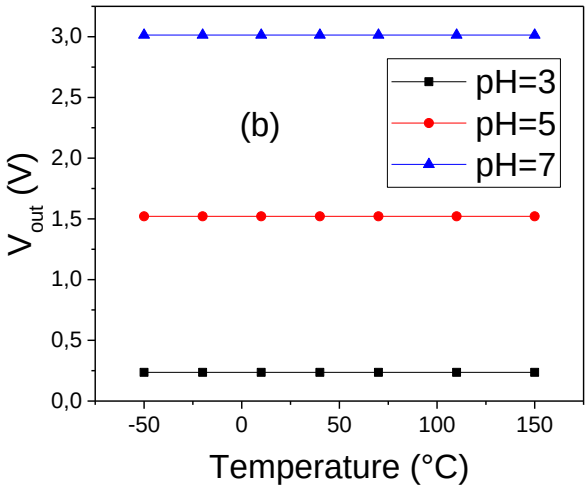


Figure 10. (a)V_{out}as a function of V_{pH} for different temperatures, (b) V_{out} as a function of the temperature.

By analysing figure 10 (b), the temperature dependency is estimates about of 2.410^{-9} V / ° C in pH =7 for temperature ranging from -50 to +150 °C. Here with this circuit the temperature has no significant interference with the output signal, before the proposed circuit, the temperature dependence of the floating-gate-ISFET is about of 6 mV/°C, and after we add the proposed circuit the temperature decrease severely and the output signal is temperature independent. All components present in figure 9 are temperature depending. Table 2 compares this work with a previous work in terms of temperature compensation. The results extracted from figures 10 are compared with other works in terms temperature dependency. Refers to table 2 the prosed circuit give a sophisticated and efficient solution for chemical sensing. Target applications can include diagnostics based on DNA detection surveillance. Thanks to the possibilities for H+ ion detection, this circuit will provide opportunities in the field of Lab-on-Chip design and chemical sensing systems.

Table2. Comparative study for temperature compensation

References	**[38] (2014)**	**[39] (2018)**	**[40] (2018)**	**[41] (2020)**	**[42] (2020)**	**[43] (2020)**	**This work**
configuration	Differential measurement	Differential measurement	Differential measurement	Differential measurement (ISFET/ReFET)	Single measurement	Single measurement (ISFET)	Single measurement (Floating-Gate-ISFET)
Technologies	ISFET	ISFET	ISFET	ISFET/ReFET	FDSOI-ISFET	ISFET	Floating-Gate-ISFET
Process	(AMI 1.0µm)	AMS (0.35µm)	(AMI 1.0µm)	TSMC (0.18 µm)	FDSOI	TSMC (0.18 µm)	TSMC (0.18 µm)
Power supply	--	3.3 (V)	--	1.8V	1.8V	1.8 V	3.3(V)
Temperature range	[20°C, 60°C]	--	[20°C, 120°C]	[0°C, 50°C]	[0°C, 50°C]	[-20°C, 150°C]	[-50°C, 150°C]
Temperature coefficient	28 10^{-6} (V/°C)	0.25 10^{-9} (A/°C)	23.37 10^{-6} (pH/°C)	5 10^{-6} (V/°C)	0.7 10^{-6} (V/°C)	13 10^{-6} (V/°C)	2.4 10^{-9} (V/°C)

V. Conclusion

In this work we validate for the first time the floating-gate-ISFET macro-model on TopSPICE with experimental data. The second part of this work is to investigate for the first-time the temperature dependency of floating-gate ISFET and we found that almost 35 % percent of the sensitivity is affected by the temperature. with that being mentioned, the third part of this work is consist to prose a robust solution to compensate the temperature effect on the output signal. In fact in the third part we propose a new circuit that is based on FG-ISFET/ReMOS topology, after that we tested the proposed circuit under temperature range goes from -50 C to +150°C and we found that the temperature dependency is about of 2.4 10^{-9} (V/°C) for pH=7.

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