VHDL Modeling of the CSMA/CA

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Abstract— The wireless communication is highly deployed due to it convenience of mobility. The wireless local area network, WLAN is dominated by IEEE802.11 standard. All the new notebooks are equipped with the IEEE802.11 b WLAN. It becomes one of the main focuses of the WLAN research. Most of the researches are simulation based due to high cost required for the hardware implementation. The IEEE802.11b standard contains two major operations, the Distribution Coordination Function (DCF) and Point Coordination Function (PCF). The main core of the IEEE802.11b, the CSMA/CA and the IEEE802.11b Physical and MAC are modeled in this paper using VHDL. The VHDL is defined in IEEE as a tool of creation of electronics system because it supports the development, verification, synthesis and testing of hardware design, the communication of hardware design data and the maintenance, modification and procurement of hardware[2]. The CSMA/CA is modeled to 3 major blocks in VHDL, the CSMACA, Random Generator and counter. The CSMA/CA is successfully modeled with a total of 58 pins and it used 15% of the total logic elements of the APEX^{TM} 20KE FPGA. The CSMA/CA can support the operation frequency up to 50MHz.

Keywords— CSMA/CA, DCF, IEEE802.11b, Wireless LAN

I. INTRODUCTION

A S technology advancement in the 21st century wireless communication had been the most popular choices of communication. More and more people are tuning into wireless due to the convenience of mobility. Although wireless communications are considerably advance nowadays, but continuous researches and developments are essential requirements to bring wireless communication performance a leap further forward. The VHDL (Very High Speed Hardware Description Language) is defined in IEEE as a tool of creation of electronics system because it supports the development, verification, synthesis and testing of hardware design, the communication of hardware design data and the maintenance, modification and procurement of hardware[2]. It is a common language used for electronics design and development prototyping.

IEEE802.11b is one of the many standards for wireless communication in the radio frequency range. IEEE802.11b defined the Medium Access Control layer (MAC) for wireless local area networks [1]. The lower sublayer of the MAC protocol is the Distribution Coordination Function (DCF) that utilizes the random access method of carrier sense multiple access with collision avoidance (CSMA/CA) to support asynchronous date traffic. Since random access is not appropriate for real-time periodic traffic, a scheduling technique called the Point Coordination Function (PCF) is implemented on top of DCF to support real-time traffic, based on polling that is controlled by a centralized point coordinator.

There are few CSMA/CA protocol had been model [4] [5], but the ways and purposes of model CSMA/CA protocol are unlike ours. Modeling CSMA/CA protocol with VHDL allowed us to build up a software component that is ready-to-used in wireless development prototyping. This could be conveniently being used as a substitution of hardware and consequently to cost reduction.

II. IEEE802.11B MAC LAYER

This paper is focusing on the CSMA/CA, thus PCF will not be discussed further in this paper. The DCF define in [1] is based on the CSMA/CA protocol. A station with a packet to transmit will sense the transmitting medium by checking the energy level and the carrier frequency for activity until an idle period equal to a Distributed Interframe Space (DIFS) has been observed. In case the medium is sensed busy, a random bakeoff interval is selected. The bakeoff time counter is decremented as long as the channel is sensed idle, stopped when a transmission is detected on the channel, and reactivated when the channel is sensed idle again. The station waits for another DIFS when the backoff time reaches zero before the station transmits as shown in Fig 1. The medium have to be idle for the period else the backoff time counter will kick off again. In addition, to avoid channel capture, a station must wait a random backoff time between two consecutive packet transmissions, even if the medium has sensed idle within the DIFS time.

The DCF adopts an exponential backoff algorithm. Backoff is a well known method to resolve contention between different stations willing to access the medium. The method requires each station to choose a random number and waits for this number of time slots before accessing the medium. Each Time Slot is equal to the time needed at any station to detect the transmission of a packet from any other station. It accounts for the propagation delay, for the time needed to switch from the receiving to the transmitting state (RX-TX-Turnaround-Time), and for the time to signal to the MAC layer the state of the channel (Busy-Detect-Time).
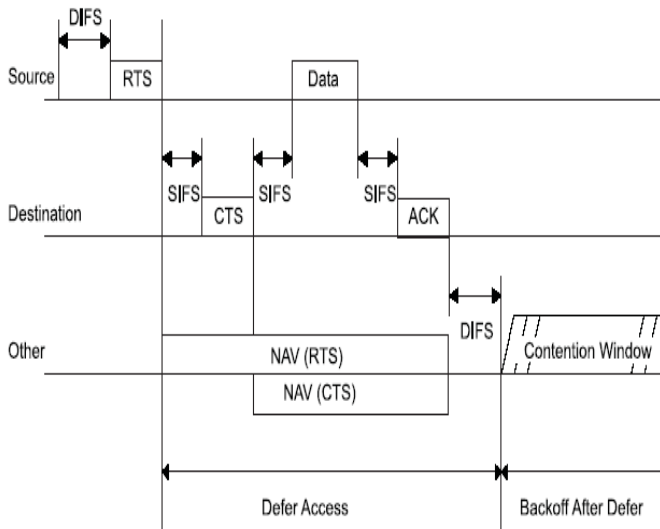
Fig 1: CSMA/CA handshake protocol.

CSMA/CA does not detect a collision by hearing own transmission [3], thus a positive acknowledgement is transmitted by the destination station to indicate the successful packet transmission. The acknowledgement (ACK) is transmitted after a Short Interframe Space (SIFS) subsequent to a received packet. If the transmitting station does not receive the acknowledgement within a specified ACK-Timeout, or it detects the transmission of a different packet on the channel, it reschedules the packet transmission according to the previous backoff rules.

The DCF protocol includes a fragmentation mechanism, which allows the MAC to split a MAC Service Data Unit (MSDU) into smaller MAC level frames, the MAC Protocol Data Units (MPDU) if the MSDU size exceeds the maximum fragmentation threshold. The different fragments are then transmitted in sequence, with only a SIFS between them. Only the first fragment must contend for the channel access. The process of recombining the MPDUs into single MSDU is defined as defragmentation. In our modeling, we assumed no MSDU fragmentation or defragmentation thus the size of MSDU and MPDU are fixed.

The standard defines an addition mechanism of four-way hand shaking to be optionally used during the fragmentation. This mechanism requires the transmission of special short Request To Send (RTS) and Clear To Send (CTS) frames prior to the transmission of the actual data frame. The RTS frame is transmitted by the source station which needs to transmit a packet. When the destination station detects an RTS frame, it responds, after a SIFS, with a CTS frame. The transmission will only start after the CTS frame is correctly received. Moreover, the frames RTS and CTS carry the information of the duration of the packet to be transmitted. This information can be read by each station, which is then able to update their Network Allocation Vector (NAV) containing the information of the period of time in which the channel will remain busy.

III.   DISTRIBUTION COORDINATE FUNCTION

The Distributed Coordination Function (DCF) is one of coordination functions which are defined in the IEEE 802.11 MAC/PHY standard. In DCF, STAs contend for the use of the channel in distributed manner via the usage of the Carrier Sensing Multiple Access with Collision Avoidance (CSMA/CA) protocol. Retransmission of collided packets is managed according to the Exponential Backoff Algorithm. In addition, all directed traffic uses immediate positive acknowledgment (ACK frame) where retransmission is scheduled by the sender if no ACK is received.

Upon receiving the RTS frame, the destination STA waits for a SIFS before sends back a CTS control frame to the requested STA or sources STA. This control frames indicates that the destination station is ready to receive data.

After waiting for a fair amount of time equal to SIFS preceding the received CTS from the destination STA, the source STA starts to transmit its data frames. When the destination STA completely received the data frame from the sources, destination STA waits for another SIFS prior to sends back an acknowledgement frames to the source STA to show that the frame has successfully been received. ACK frame also carries the flow control information with it to the source STA.

IV.   DCF ACCESS PROCEDURES

Whenever a STA want to send a frame, the source STA senses the medium by checking the energy level at the carrier frequency. The STA uses a persistence strategy with backoff until the channel is idle. After the STA found idle in the medium, the STA waits for a DIFS. If there is no disturbance in the medium for more than the duration of DIFS, the STA sends a request to send (RTS) control frame to the destine receiving STA, else, the source STA will have to go through the persistence strategy with backoff until the channel is idle again. Fig 2 shows the exchange of data and control frames in time for a complete virtual carrier sense handshake mechanism.

V. WIRELESS PHYSICAL CONTROL MODULE

CSMA/CA module is a model of a protocol interactively related with the physical layer of the wireless devices. This includes NAV value, idleness of the medium, receiving of the CTS or ACK frames from the receiver. All these features are relayed to the CSMA/CA module so that proper protocol responses are conducted by the CSMA/CA module. Thus, together with the complete CSMA/CA model, an extra module is connected to the CSMA/CA module in order to provide proper PHY response related to the request. This extended module is called the wireless PHY control module.
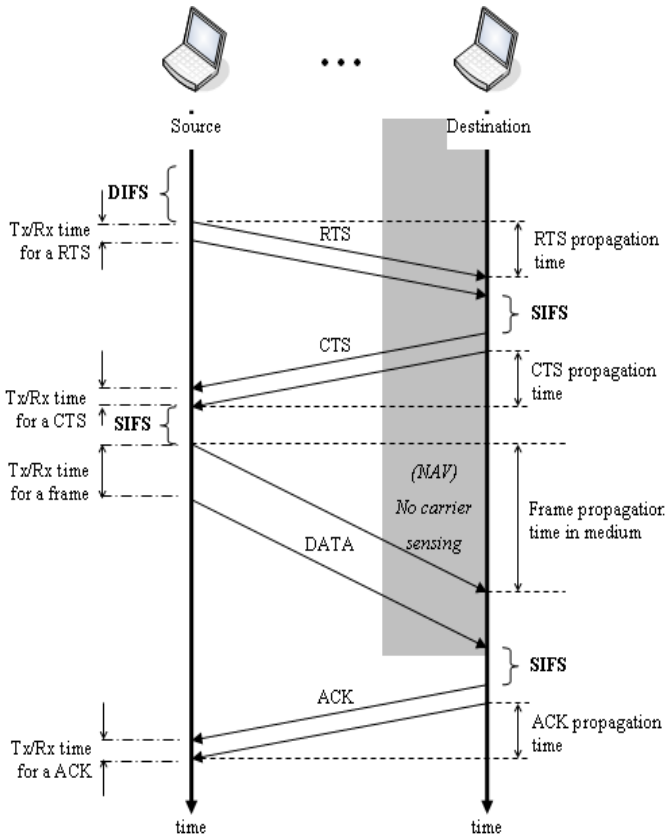
Fig 2: CSMA/CA frame exchange time line

Fig 3: The Wireless PHY Control Module

This interactive module is developed for the following reasons.

- To provide any possible responses emulating the PHY to the CSMA/CA module so that the CSMA/CA module could be tested for its competence in ideal case.
- To test the timing responses of the CSMA/CA module.
- To send indication of the frame transmission complete from the PHY to the CSMA/CA module.

It is impossible emulate the real PHY conditions. Therefore this module (as shown in Fig 3) is developed with the assumptions that:

- The PHY is always detected to be idle but could manually being interrupted.
- The response time for the CTS and ACK are predetermined.
- NAV is inconsistence and dependent to time.

VI.   IEEE802.11B MAC FRAME FORMAT

Each frame consists of the following basic components (shown in Fig 4):

a)   A MAC header, which comprises frame control, duration, address, and sequence control information.

b)   A variable length frame body, which contains information specific to the frame type.

c)   A *frame check sequence* (FCS), which contains an IEEE 32-bit *cyclic redundancy code* (CRC).
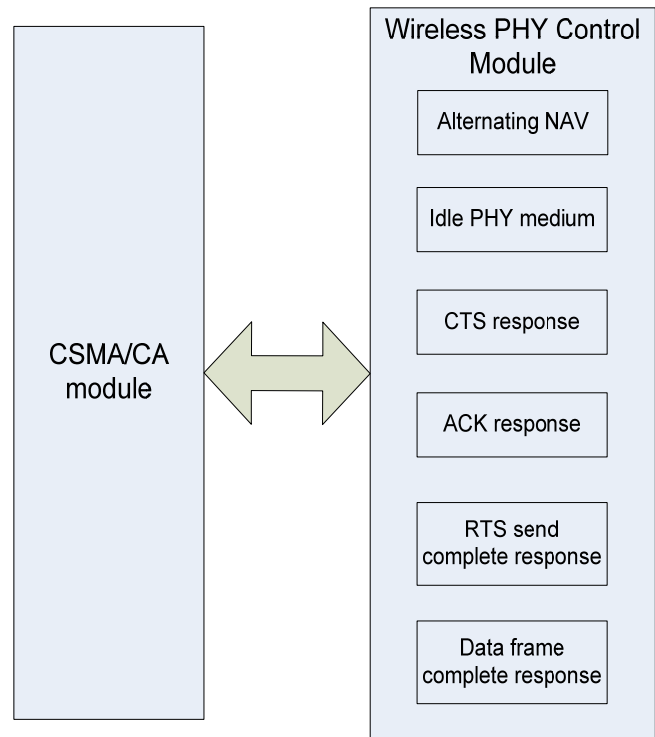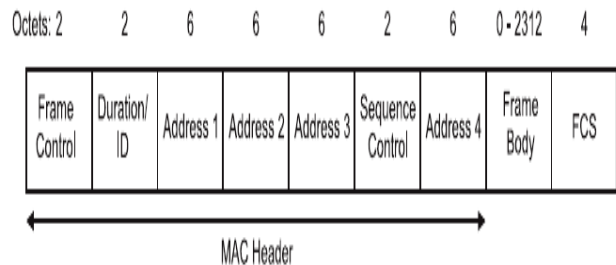

Fig 4: General MAC frame format [4]

VII.   VHDL MODELING OF CSMA/CA

The Altera's Excalibur embedded processor solution [6] which integrates an industry-standard ARM922T™ processor with debugging modules, on-chip memory, and peripherals with an APEX™ 20KE device-like architecture is used as the target device for simulation analysis. This combination provides system performance of up to 200 MHz (210 Dhrystone MIPS) and an FPGA with embedded RAM, phase-locked loops (PLLs), and advanced I/O capabilities. Quartus® II design software is used for the simulation analysis.

The CSMA/CA handshake system (Fig 5) model contains 3 major modules which are CSMACA, Random Generator, and counter. The CSMACA module is the major module block that holds the behaviors of the CSMA/CA protocol. A total of 58 pins are used with 2 pins are assigned as global pins, the clock (clk) and the reset, 8 pins for passing the random generate value from random generator (RandomVal) into

CSMACA module, 32 pins are used to pass integers value (countStop_val) out from the CSMACA module to the counter and the remaining 16 pins are I/O pins that interact with other module. This module uses 15% of the total logical element that is supported in APEX™ 20KE FPGA.

The counter module accepts value of unsigned integers from CSMACA module and start counting. After it counted for the assigned times of count, it return a trigger to indicate to CSMACA module that the count is done. While the counter module is trigger to start, CSMACA module will goes in to waiting state. The main functionality of this counter module in this system is to count the waiting time with respect to the clock speed used. The time duration from the start count till end count will be the time that the integer value assigned multiply by the clock speed used.
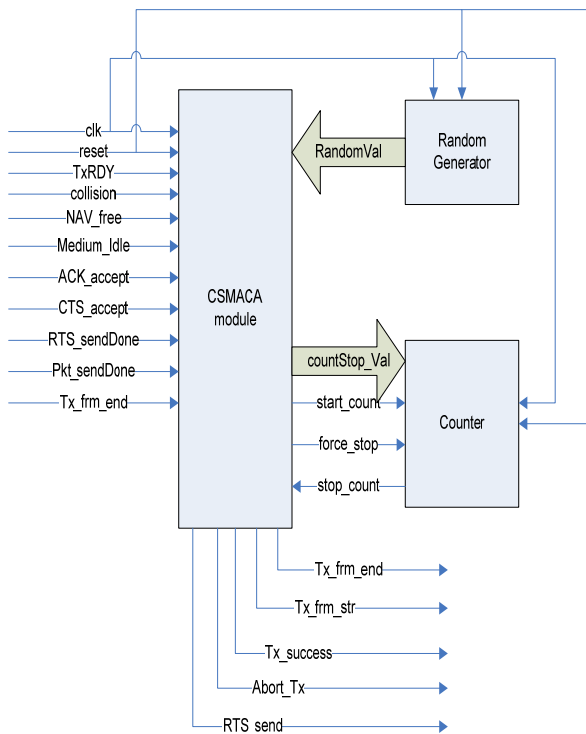

Fig 5: Block diagram of IEEE802.11 MAC Layer CSMA/CA protocol model with VHDL.

The random generator supplies the CSMACA module a random value of integer from the range of 7 to 255. This random value is used in Backoff after a packet is successfully transmitted. The Backoff time is uniformly chosen in the interval (0,CW-1) defined as the Backoff Window (Contention window) [1]. At the first transmission attempt, CW = CWmin, and it is doubled at each retransmission up to CWmax. The values suggested in the draft standard [1] are CWmin = 7 and CWmax = 255.

CSMA/CA model could support an operation frequency up to 50 MHz since 20ns clock period is used for the simulation. This operation frequency is very much higher the channel bit rate. As the value of the ACK-Timeout is not specified in the standard, it has been chosen sufficiently long (300 µs) to contain a SIFS, the ACK transmission and a round trip delay. The others parameters such as, SIFS, DIFS, ACK timeout time RTS timeout time, channel bit rate, packet size and etc. which are used in our model are listed in the Table 1.

Table 1: Parameters used in modeling

Packet Payload	88 Bytes	DIFS	50 µs
RTS Payload	20 Bytes	SIFS	28 µs
CTS Payload	14 Bytes	ACK time out	300 µs
ACK Payload	14 Bytes	RTS time out	300 µs
Channel Bit Rate	11Mbps	CTS time out	300 µs
Tx Rx Round Trip Time	20 µs	Propagation Delay	1 µs
Slot Time	50 µs		

VIII. SIMULATION RESULTS OF RANDOM GENERATOR MODULE

Fig 6 (a) and (b) are a continuous waveform results of the module, but it is cropped in two defining moment in time due space consumption. Fig 6 (a) exhibits the incremental count of output, the "randonVal". Marker (1) shows the width of every count is at one clock cycle. Thus, the module incrementally counts until it reaches the threshold value of 255 and then returns back to the lowest value and continues. This repeatedly incremental count process is indicated by marker (2) in Fig 6 (b). The output values are continuously fed to the CSMACA module once system clock starts except for resets.

IX. SIMULATED WAVEFORMS RESULTS OF MULTI_COUNTER MODULE

The Multi_counter is a counter that counts for the value that is fed to it, and returns a count end signal once count ended or stops counting with the request from the CSMACA module.

Fig 7 is the resulted waveform from the Muilti_counter module. It is divided into four parts which simulated the possible response that this module could provide. Part A is actually an ideal case for the multi_counter. The module retrieved a value that is fed in through count_val in port concurrently when the str_count is set, indicated at (1). (3) shows the duration for a 16 clock-cycle-count. A signal is sent thought end_count output port after finish counting. Part B shows the situation where multi_counter is terminated with the signaling of killTimer inpot port. At Part C, the multi_counter is set to count for 20 clock cycle. The duration, indicated at (4) is longer with compare to (3). This proves that the multi_counter actually counts and the time used to count is proportion with count_val and system clock cycle period. Part D shows that whenever there is count on going, the multi_counter will be terminated when an interrupt is detected. The value of count_val in this simulation is used for the purpose of testing the functionality of this multi_counter module.
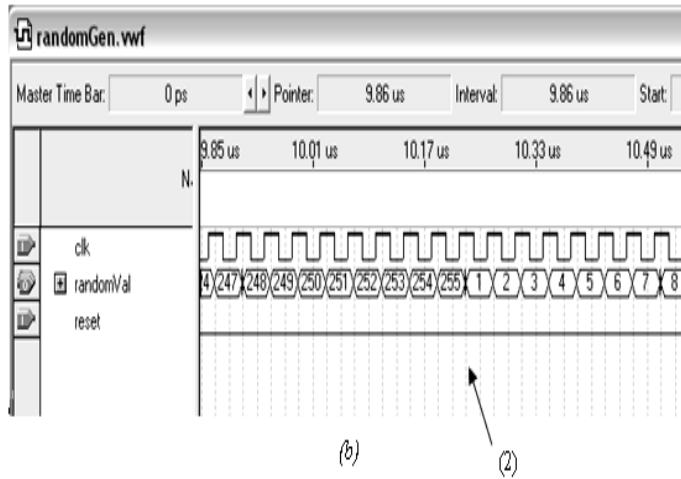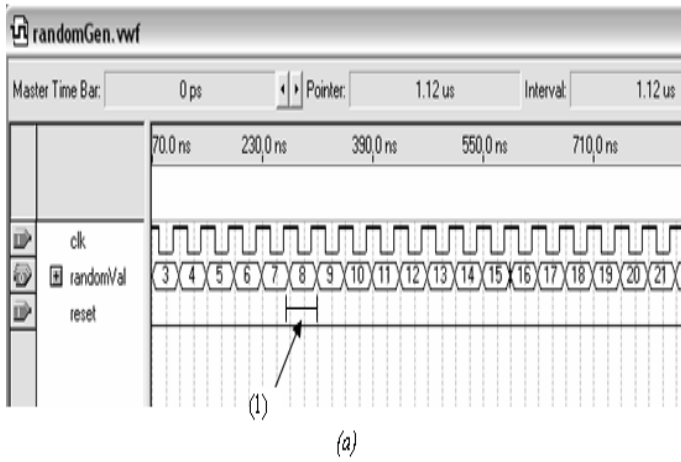
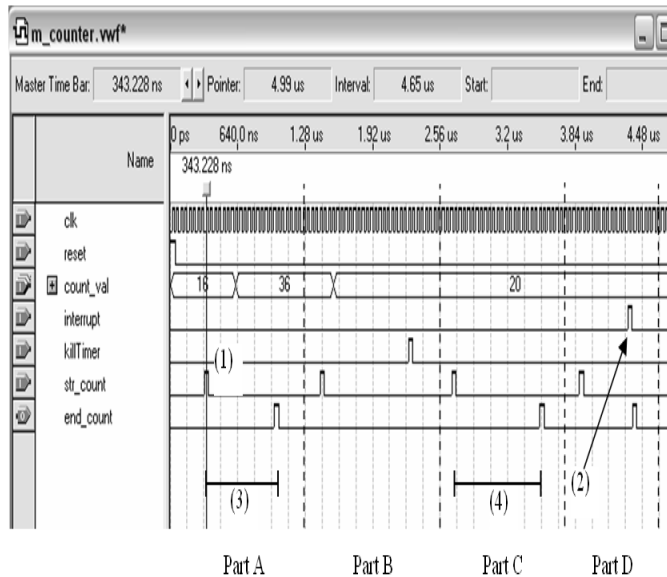Fig 6: Simulated waveform results of Random generator module

Fig 7: Simulated waveform results of Multi_counter module

X. SIMULATION RESULTS OF CSMA/CA

The transmitting packets are of fixed length and the time to transmit a packet is by dividing the packet payload with the channel bit rate for IEEE802.11b in the CSMA/CA protocol VHDL modeling.

Each packet to be transmit is assumed to be stored and waiting outside of this system. Then whenever there is signal from TxRDY input pin, which indicate there are packet ready to be transmit, the CSMA/CA will start checking the NAV and will start sense for idle medium if the NAV is equal to zero. If the medium is idle for duration of DIFS time, then the handshake protocol starts as shown in Fig 8.

Handshake protocol starts by sending out a RTS frame to the receiving side. The time for transmitting a RTS frame will be the RTS payload size divided by the channel bit rate. When RTS frame is fully send out, CTS time out timer starts to count as shown in Fig 9. If CTS frame is not received before the counter ends, it could be the CTS had been lost in transmission or there is a hidden node problem, then backoff is kick started and the backoff value will double the previous value. But, if CTS frame is received before the timer ends, it indicated medium is safe to transmit. The packet that is waiting is sent out to the PHY with Tx_frm_str pin set to high. Similarly the time to transmit out a complete frame out of the transmitting station is the ratio of packet payload and the channel bit rate. Once the packet is completely sent out, an ACK time out timer is triggered start. The next state of process is depended on weather ACK frame is received before ACK time out. If the transmitting station does not receive the ACK frame on time, the backoff will be called again and transmission is tried again after the backoff time count ends. However, ACK frame indicates the success of packet transmission if it is received before time out.

Upon successful transmission, Backoff will be assigned a random value from the Random Generator (Fig 10). This backoff value holds back the immediate successful station to allow other stations in the network to use the medium, avoiding channel capture by a particular station.
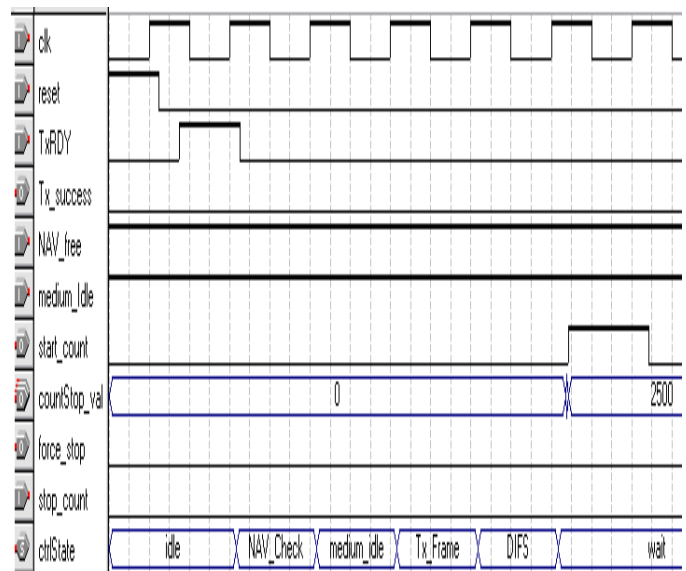

Fig 8: Simulation indicates triggering of CSMA/CA handshake protocol with TxRDY pin.
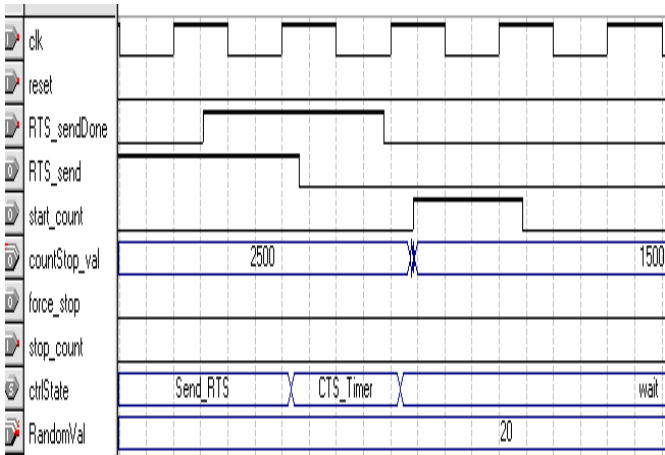
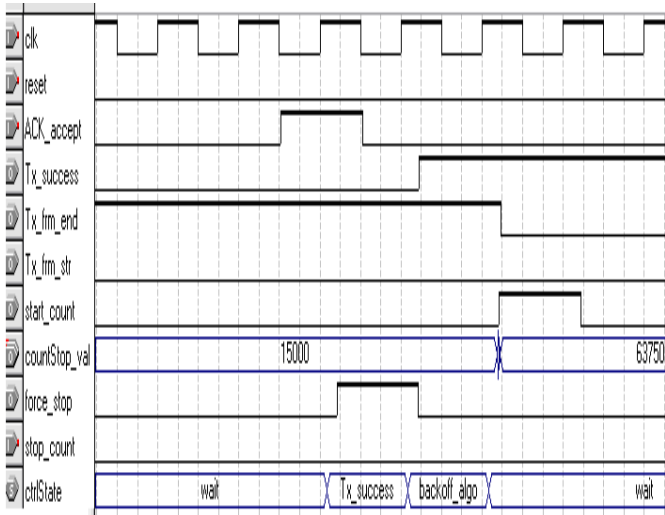Fig 9: Simulation output on CTS time out count starts after RTS packet was send.

Fig 10: Simulation exhibits the backoff taken after any successful frame transmission.

XI. SIMULATION RESULTS OF DCF MAC

The complete module (Fig 11) with the coagulation of CSMACA module, Multi_counter module, Random generator module and the wireless PHY control module. The results that are being displayed in this section have the combinational characteristics of all modules. Their functionalities are the same, however the timing responses are more accurate and the responses are based on predefined values stated in Table 1.

Fig 12 and Fig 13 displayed the results of the simulated waveform results of the complete MAC model characteristics with true simulate timing responses. The waveform is divided in to two parts. There are Part A and Part B. Both parts are actually similar, they portray two successful transmissions of frame individually. But this figure defined the functions of backoff after ever successful transmission of frames. A random backoff do occur intermediately of Part A and Part B. The Part A and Part B are covered the eight major parts each in the simulation analysis. The eight major parts are shown in

Table 2 and the Part A result can be analysed in 8 major individual parts as shown in Fig 14.
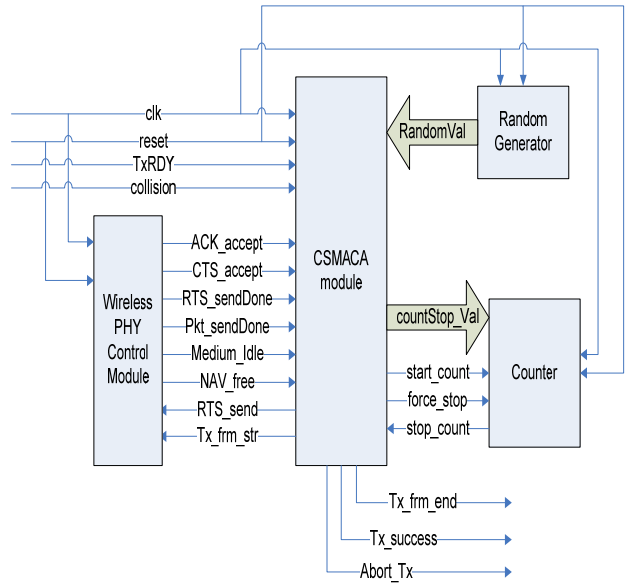

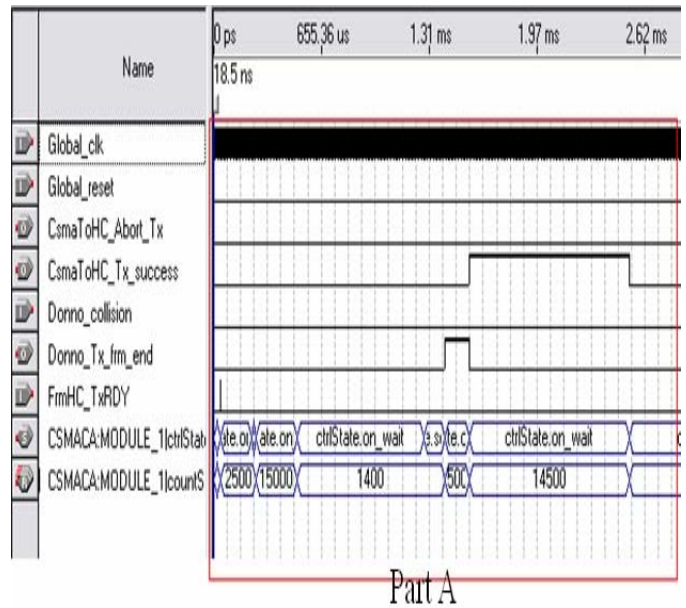Fig 11: Block diagram of integration of modules

Fig 12: Simulated waveforms results of Complete CSMA/CA model (Part A)

In the timing log of Quartus II timing analyzer, the worst case scenario for the global clock is 19.37 MHz (period = 51.634 ns). Under the worst case timing of this MAC model, yet the value is still greater than the required frequency. From compilation summary report of Quartus II, the MAC model uses only 8% of the total numbers of logic elements in and 1% of the total pins provided by the device. This means that the module is compact enough to surf as software tools used on future wireless development.
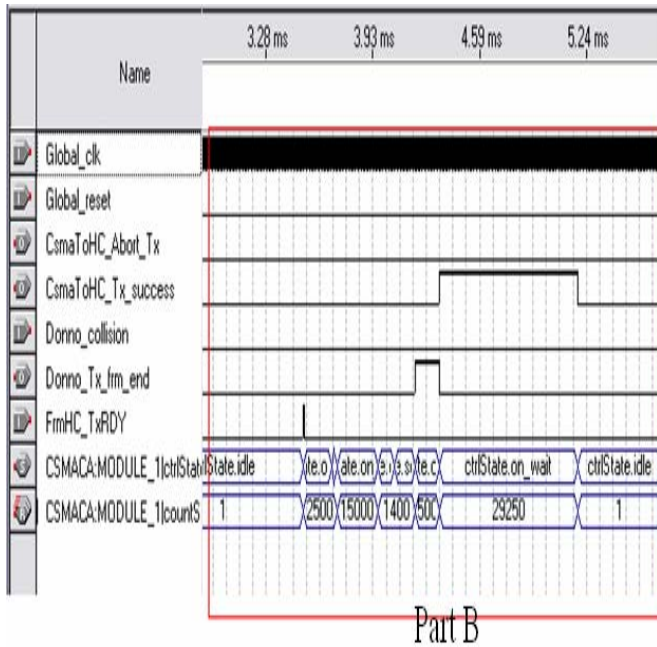
Fig 13: Simulated waveforms results of Complete CSMA/CA model (Part B)

Table 2: The 8 major simulation analysis

1	CSMACA module sensed the medium and waited for DIFS
2	Medium is Idle for more then DIFS. Proceed to the sending of RTS frame.
3	RTS is fully transmitted out. CTS timer is activated and starts counting
4	CTS frame was received before the CTS timer expired. This continues with SIFS wait.
5	After SIFS, CSMACA module sends out the data frame.
6	Once the data frame is complete sent out from the transmitter, ACK timer starts awaiting ACK
7	ACK frame is received. Random backoff start counting
8	Random backoff complete. CSMACA module returns to Idle state awaiting the next TxRDY signal.

Fig 14: Simulation result of the 8 major operation of the CSMA/CA (Part A) result

XII. CONCLUSION

A compatible IEEE802.11b MAC Layer CSMA/CA handshake protocol is successfully modeled in VHDL. As VHDL is commonly used in industry for prototyping hardware, our model could be applied directly to the prototyping with great portability. The Physical layer is modeled for a more complete simulation analysis. In future works, we will expend the model with NAV with frame detector, Encryption, Management module, Spanning Tree Protocol, Learning Tree Protocol and Header Converter modules. Constantly model until we could construct a complete VHDL wireless access point system.
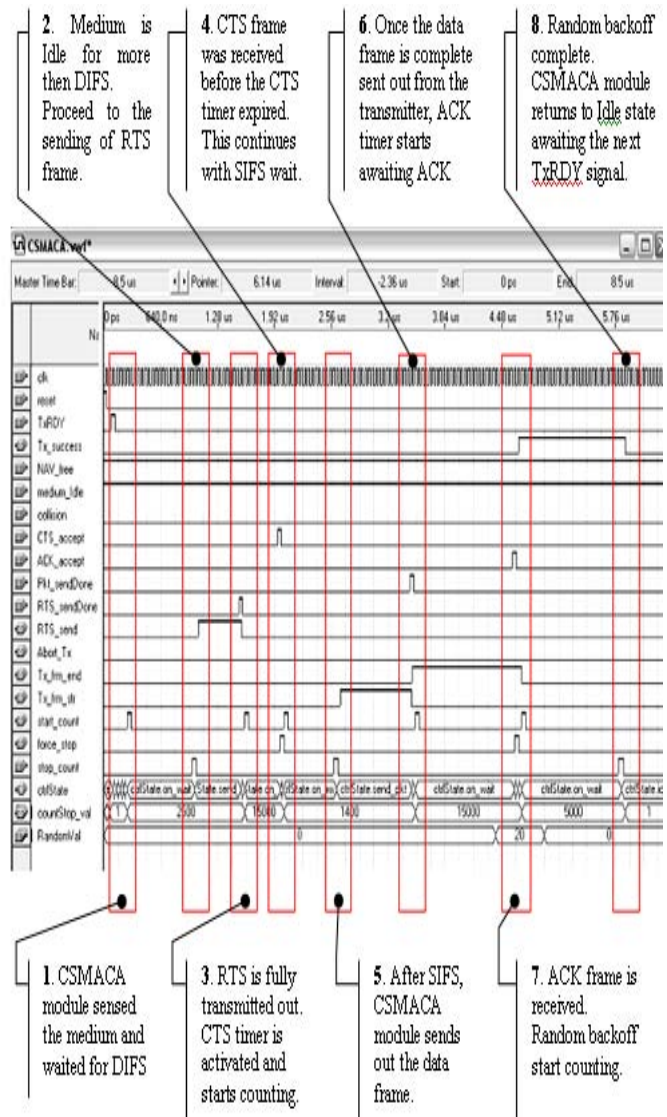
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