Muli-threshold low power Shift Register

SAMEH ANDRAWES, LEILA.KOUSHAEIAN, RONNY VELJANOVSKI

***Abstract*—**This journal focus on the design of the shift register in the sub-threshold region of the transistor which is called the weak inversion. In the weak inversion region of the transistor, the voltage supply is less than the threshold voltage of the transistor to minimise both of the dynamic power (while the circuit is in an active mode) and the static power (while the circuit is in the stand-by (idle) mode). The weak point of the operation of the transistor in the weak inversion region is that; the circuit operates more slowly compared to the high voltage supply design (where the transistor is in the strong inversion region). so this technique is useful for the low frequency operations mainly. We present the design and implementation of a low power Complementary Metal Oxide Semiconductor (CMOS) ten-bit shift register by using negative latch D Flip-Flop (DFF) in the sub-threshold region (weak inversion region) with relatively high speed in the active mode and low power consumption during the sleep mode (idle mode) using Multi-threshold Complementary Metal Oxide Semiconductor (MTCMOS) technique. The circuit was implemented in 90 nm from STM CMOS technology, with oxide thickness of $16A^0$, 250 mV power supply, 5 MHz clock frequency with 10 % activity (the circuit is in the active mode fore 10% of the clock frequency and in the idle mode for the rest of the clock frequency time), average power consumption is 6.43 nW and power delay product "PDP" (the multiplication of both of the total power consumption and the propagation delay) is 24.43 aJ. The shift register has been designed and simulated by using Cadence tools.

***Keywords*—**leakage, low power, MTCMOS, Sub-threshold, Shift register.

I. INTRODUCTION

ow power design is a very important topic nowadays because of the battery life time, so the electronic circuit designers are worried nowadays about decreasing the total power consumption to increase the battery life time [1] especially for the portable embedded system [2] and decrease the battery's size which is reflected on the portability of the devices like the Lap-Top computers and Cellular phone. The deep sub-micron technology makes the leakage current, the dominant one which was ignored in the past. Long battery life time can be obtained by minimising the total power consumption. Most of the electronic components recently have two modes; active mode and stand-by mode [3]. In the active mode, the circuit executes a certain operation while in the

stand-by mode (idle mode), the circuit is doing a non-performance critical operations, Like ATM machine waiting for an input from the customer. There are different techniques to do that while the most effective way is the low voltage supply level.

$$P_{dynamic} = C * V_{dd} * f_{clk} \quad (1)$$

Equation (1) represents the dynamic power consumption which is due to charging and discharging the parasitic and output load capacitances. The dynamic power is directly proportional to the supply voltage, load capacitance and frequency, so to minimize the dynamic power consumption, the circuit must be loaded with low capacitances (depends no the load), supplied through low voltage source and operate at low frequency (while some applications need high frequency "speed"). So decreasing the voltage source is one of the most effective ways to minimize the power consumption.

$$T_{pd} \alpha V_{dd} / (V_{dd} - V_{th}) 2 \quad (2)$$

As shown in equation (2), the propagation delay is reciprocal proportional to the square of the difference between the voltage source and the threshold voltage of the transistor (the threshold voltage of the transistor is defined as the gate voltage where an inversion layer forms at the interface between the insulating layer (oxide) and the substrate (body) of the transistor). So scaling down the voltage source without scaling down the threshold voltage decreases the difference and increases the propagation delay. To minimize the propagation delay, the threshold voltage needs to be scaled down to increase the difference between it and the voltage supply while Scaling down the threshold voltage 'V_{th}' is limited where making the threshold too low makes it difficult to turn off the device completely.

Figure.1 shows the trade off between the propagation delay and the power consumption where as power consumption decreases as the propagation delay increases and vise versa.

In the sub-threshold region the transistor can work properly at gate source voltage lower than the threshold voltage of the transistor ($V_{GS} < V_{TH}$), under this condition the transistor is operating in weak inversion region and the current in this

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mode is called a sub-threshold current or leakage current and its equation is

$$I_{leakage} \alpha e^{(Vgs - Vt)/Vth} \quad (3)$$

where V_t is the thermal potential.

Equation (3) shows the relation between the leakage current (leakage current is the current in the CMOS transistor while it is in off state (ideal mode) due to different mechanisms which are sub-threshold current, gate leakage current, reverse-bias p-n junction current, gate-induced drain leakage (GIDL) current, and finally punch-through current) and the threshold voltage of the transistor. It is clear from equation (3) that the leakage current is exponential proportional to the threshold voltage. The problem is that as the device threshold decreases the leakage current increases [5] [8] which leads to increase the static power consumption.

$$P_{static} = I_{leakage} * V_{dd} \quad (4)$$

Equation (4) illustrates that the static power consumption (power consumed during the stand-by mode) is directly proportional to the multiplication of the leakage current and the voltage source. This power was neglected for the high threshold technology but for sub 100 nm, it becomes a dominant part of the total power consumption which could be even more than the dynamic power especially for the devices which are, for the majority of the time, in the stand-by mode, such as cell phones [9].

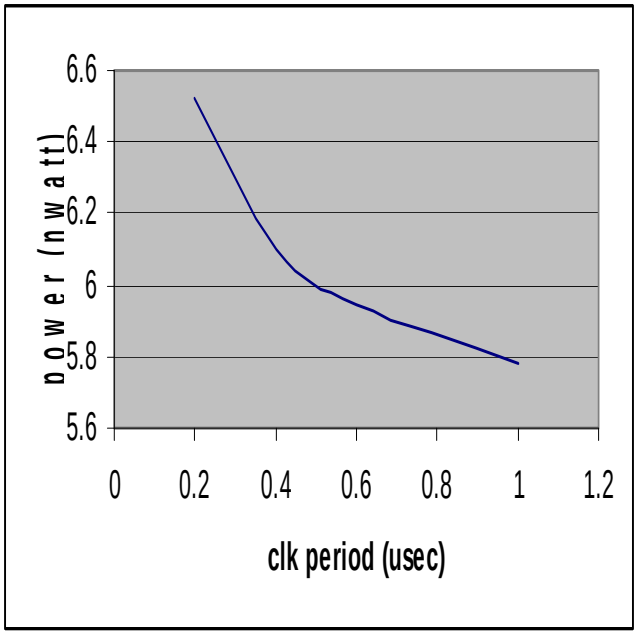

Fig.1 Trade off between the power consumption and the propagation delay.

$$P_{total} = P_{dynamic} + P_{static} \quad (5)$$

Equation (5) shows that the total power is the summation of the dynamic and static power which indicates that scaling down the voltage source leads to lower the total power consumption.

As the circuit spends more time in the ideal (stand-by) mode, so it is practical to reduce the leakage current to minimise the static power which represents the dominant part of the total power consumption. Multi-threshold CMOS (MTCMOS) technology is one of the most effective techniques to reduce the leakage current during the standby mode by using a low threshold voltage transistor in the critical paths of the circuit to improve the performance while the high threshold voltage one is in uncritical paths and is used as an isolation switch between the virtual supply lines (Vdd, GND) and the real one [8].

It is important to minimize the voltage supply to reduce the power consumption (advantage) while the maximum frequency is reduced also (disadvantage), so there is always trade-off between the power consumption and the speed. In the sub-threshold region the speed of transistor is very sensitive to the supply reduction where the delay $\propto$ (supply/ e^{supply}), so as voltage supply decreases as the delay increases dramatically. Scaling the threshold voltage of the transistor is limited where making the threshold too low makes it difficult to turn off the device completely and some of intrinsic device voltages are material parameters and can not be scaled. Scaling down the voltage is required but not easy. The scaling of the supply voltages is critical for low power operation without the scaling of device threshold otherwise the device does not function properly. So low supply voltage requires the use of low threshold devices.

Section 2 presents designing the low and high threshold inverters in sub-threshold region. The basic core of DFF negative latch is presented in section 3. The implementation of the shift register is illustrated in section 4 which can be used in CMOS wireless sensor applications and in the Analog Digital Converter (ADC) based on the Successive Approximation Register (SAR) [13], [14]. The results and simulations are discussed in more details in section 5.

II. Optimized Sub-Threshold Inverter

Operating the static CMOS inverter in the sub-threshold region (weak inversion region) of the transistor requires (for both PMOS and NMOS) that the input level voltage must be lower than the threshold voltage of the transistor itself. The analysis has been done for the typical process corner low threshold transistor (it is assumed that the whole die has the same density which is ideal case, where due to the fabrication

processes, the density varies across the die) where the threshold voltage for NMOS and PMOS is measured and recoded as 169.1 mV and 343.7 mV respectively (defined at drain source current I_{DS} = 1 μA). Therefore, to make sure the NMOS is in the sub-threshold region, the input level must be lower than 169 mV (when the input signal to the inverter is high), while for the PMOS the supply voltage must be lower than 343 mV (when the input signal to the inverter is low).

Minimum voltage supply operation occurs when the PMOS and NMOS devices have the same current and it can be achieved through sizing the width of PMOS transistor with respect to NMOS transistor to get the same current. Fig-2 illustrates the minimum voltage level regarding to the failure points which define the output of the inverter as lower than 10% of the voltage source when the input signal is high and more than 90% of the voltage source when the input signal is low. The upper boundary on size occurs because the sub-threshold leakage through a large PMOS device limits the extent to which the smaller NMOS can pull down the voltage at the output node.

The curve denoted by WP max where the output of the inverter is lower than 10% of the supply, while the lower boundary on size occurs due to the limitation of the small PMOS to pull up the voltage at the output because of the sub-threshold leakage through a large NMOS device.

The curve marked with WP-min shows the minimum PMOS width for which the high output voltage achieves higher than 90% of voltage source; the point where the two bounds cross indicates the minimum operating voltage level and the PMOS width needed to achieve that. For a typical transistor in the 90 nm technology, the minimum operating voltage is 98 mV, and the PMOS transistor width to the NMOS transistor width sizing ratio (Wp/Wn) to achieve this minimum voltage is 3.

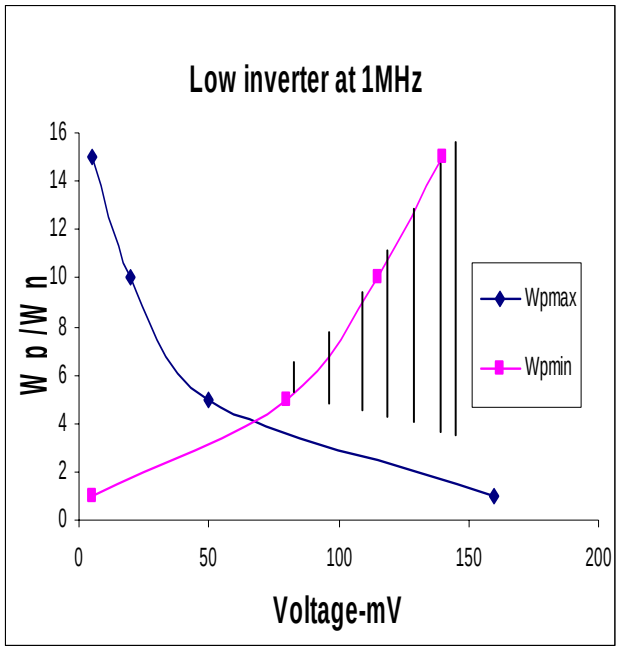

Fig.2 Sizing low threshold inverter for min V_{dd}

While minimum voltage operation occurs for symmetrical PMOS and NMOS currents, this optimum ratio indicates that the PMOS transistor width of the inverter must be 3 times the width of the NMOS to equalize the sub-threshold currents in this technology. The valid functional operation region as shown in Fig.2 is the shaded area.

The low threshold inverter operates at 98 mV voltage source, when the input signal is 98 mV and zero the output level is 2.019 mV (< 10 % Vdd) and 93.89 mV (> 90 % Vdd) respectively as shown in Fig.3.

The same analysis is used to get the aspect ratio (the width value of the PMOS transistor to the width value of the NMOS transistor) of the high threshold inverter in the sub-threshold region of the transistor where the minimum voltage supply for the high threshold inverter is 63 mV and the PMOS transistor width to the NMOS transistor width sizing ratio (Wp/Wn) to achieve this value is around 4 as shown in Fig.4.

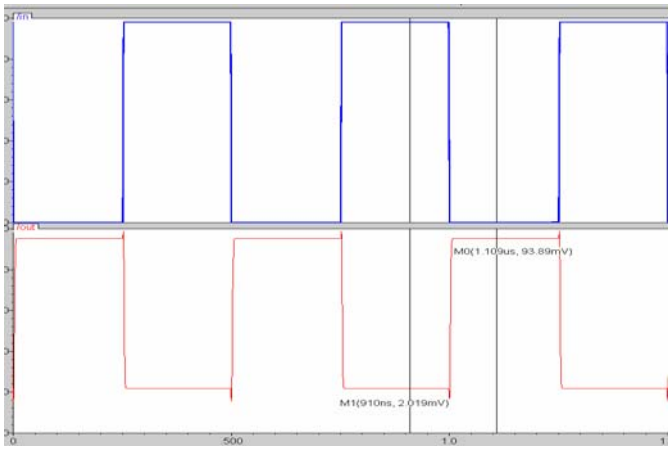

Fig.3 the output waveform of the low threshold inverter in the sub-threshold region.

The output waveform of the high threshold inverter in the sub-threshold region is shown in Fig.5.

The aim of designing both of the high and low threshold inverters in the sub-threshold region of the transistor is to use them in the design of the negative latch circuit in the sub-threshold region. So now after getting the optimum value of the aspect ratio of both of the high and low threshold inverters in the sub-threshold region, we can start by these values in the design of the negative latch circuit until getting the optimum design of the whole circuit to work properly in the sub-threshold region.

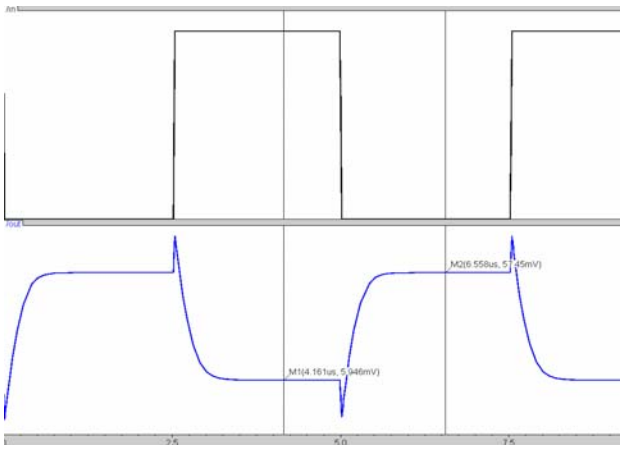

Fig.5 waveform of high-threshold inverter in the sub-threshold region.

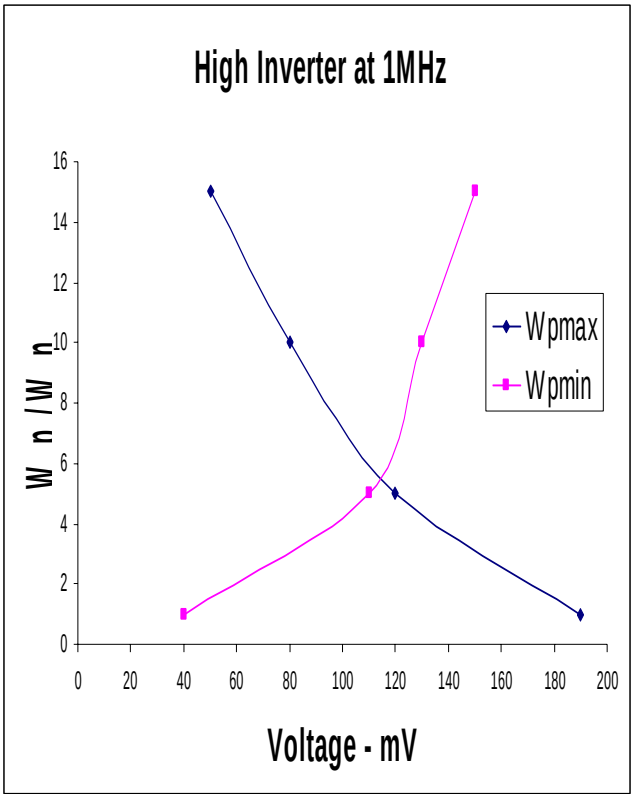

Fig.4 Sizing high threshold inverter for min V_{dd}

III. Low Power MTCMOS Latch

There are different techniques to overcome the problem of the leakage current like switch source impedance, stack effect, body biasing, Dual-threshold CMOS where the high threshold transistors are used in non-critical path and the low threshold transistors are used in the critical path to improve the performance, Variable threshold CMOS (VTMOS) Through the body biasing control where during the active mode a zero body bias is applied while in sleep (ideal mode) mode a reverse body bias is applied, Dynamic threshold CMOS (DTMOC) and Multi-threshold CMOS (MTCMOS) which is used in this projects.

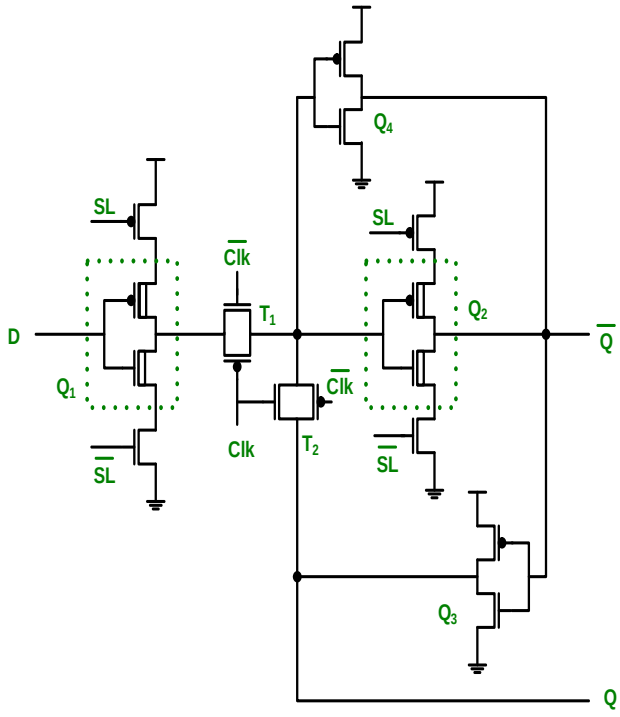

Fig.6 Schematic of the MTCMOS low power Latch

One of the most effective techniques to minimize the leakage power consumption during the standby mode of the device is Multi-threshold CMOS (MTCMOS) [6], [8], [9] where a low threshold device is used in the critical path to improve the performance while the high threshold one is used in uncritical path.

The circuit of the negative latch in the sub-threshold region has been proposed in [15] as shown in Fig.6 where D is the input signal, Q bar and Q is the output and the inverted output respectively, SL and SL bar is the sleep mode signal and the inverted sleep mode signal.

To achieve the minimisation of the leakage power during the standby mode, high threshold transistors are used as an isolation switch between the real power supply lines and the virtual lines, where during the standby mode, the sleep signal will be high (1 logic level), so the high threshold PMOS and NMOS will be switched off and the virtual power supply lines will be floated to eliminate the leakage current [10]. The high threshold inverters are used to hold the output during the standby mode (feedback circuit), as output must be valid during the sleep mode as it can represent an input to another stage. To improve the noise performance, T1 and T2 must be a transmission gate (both of PMOS and NMOS devices together) instead of a pass gate (only PMOS or NMOS device) where T1 is used to improve the metastability to ensure that the output of Q1 does not have to fight with the output of Q3 while T2 is used as a switch to open the feedback circuit during the active mode and allows output to follow input. The optimum design to eliminate the sneak leakage current is using local sleep devices [13]. Using only one polarity sleep device (whatever PMOS or NMOS) or sharing the sleep devices causes sneak leakage path and increases the leakage current when a MTCMOS gate shares the output with high threshold CMOS. Consequently, each of Q1 and Q2 must have its own sleep device and the sleep device must have both PMOS (activated by sleep signal) and NMOS (activated by the inverted sleep signal to be active during the same period in which the PMOS is active).

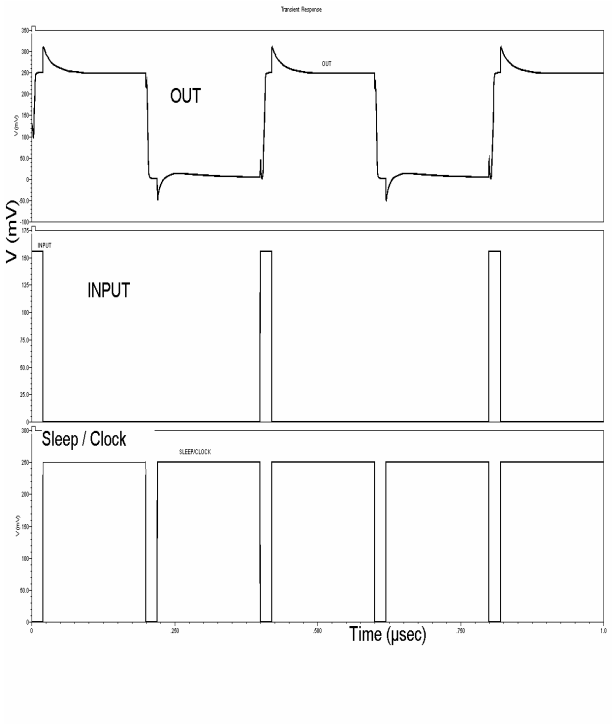

Fig.7 output following input until sleep mode activate

Fig.7 depicts that the output follows the input in the active mode (clock is low so the feedback path is open and to make the output follows the input) and the output is held in the standby mode (clock is high so there is no path between the input signal and the output one while the feedback loop is closed to hold the output) even when the input changes.

The delay of the negative latch (response of the output of the latch to the input of the latch during the low level of the clock cycle is measured between the 50% transition point of the clock cycle when it is going down "as the output is following the input only when the clock cycle" and the 50% transition point of the output waveforms respectively) is T_{delay} = 4.3 nsec as shown in Fig.8, Where the clock frequency is Freq = 5 MHZ while the rise time (time to go from 10% of the full wave to 90% of the full wave of the output) is T_{rise} = 4.1 nsec and fall time (time to go from 90% of the full wave to 10 % of the fulll wave o f the output) is T_{fall} = 3.4 nsec.

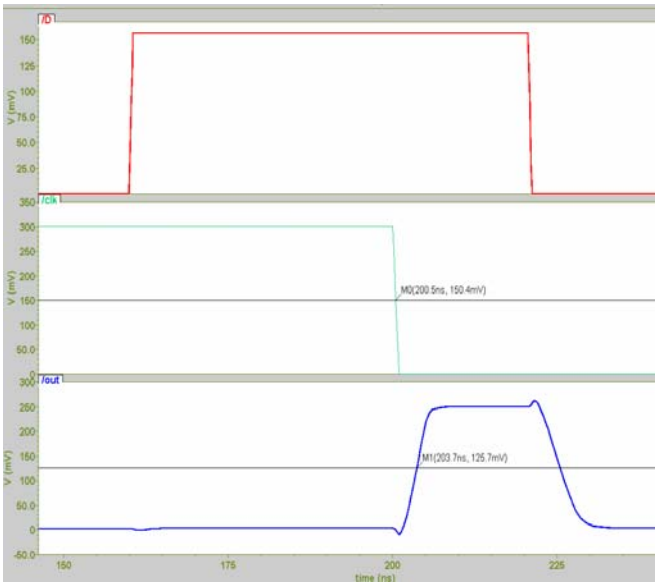

Fig.8 negative latch delay

IV. Shift Register

The shift register is the core of different circuits like the CMOS image sensor which operates at low frequency and the core of the SAR which operates at medium frequency where the low power consumption is a big issue for both.

One bit shift register is designed based on the latch described in the previous section, where to shift the input data by one clock cycle three blocks of the latch are required to be connected to each other while the middle block operates with the inverted clock of the first and last block as illustrated in Fig.9.

When clock is low the first and last latches are active while the second one is in the hold mode and when the clock is high the first and last latches are in hold mode while the second one is active by this way the input signal which is sampled during the low level of the clock and hold during the high level of the same clock is shifted by one clock cycle as illustrated in Fig.10.

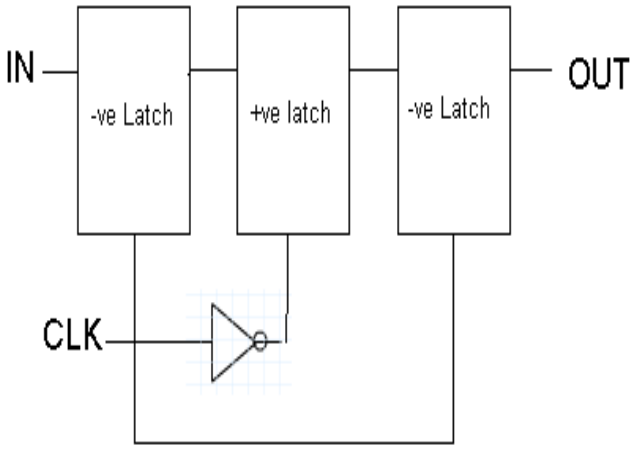

Fig.9 One bit shift register block.

For n-bit shift register, the required number of latches can be calculated from the following equation:

$$N = 2(n - 1) + 3 \quad (6)$$

Where N is a number of latches, and n is a number of shifted bits. For instance, a two-bit shift register requires five latches.

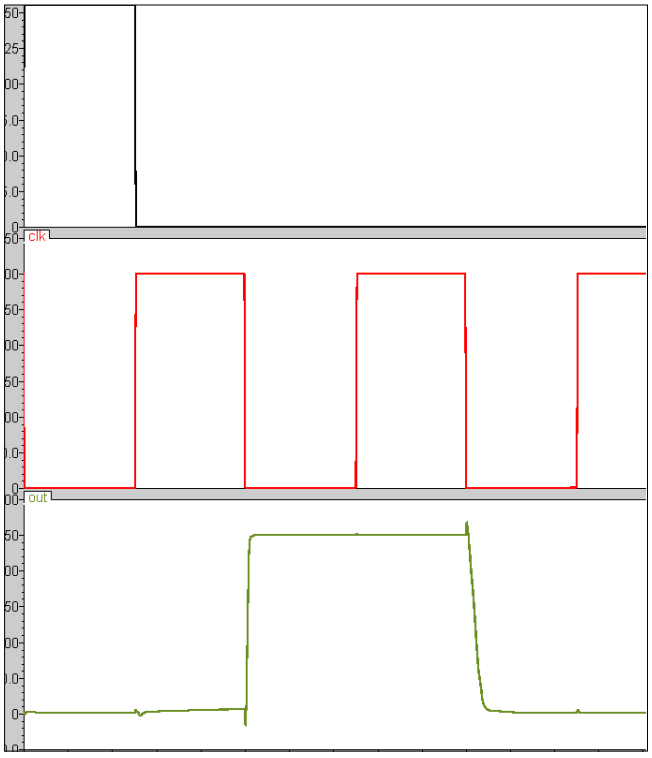

Fig.10 waveform of one bit shift register

V. Simulations

To demonstrate the significance of the power reduction, the simulation was done for 10-bit shift register. The experimental result verifies that the virtual power supply lines during the active mode and standby mode are 249.8 mV (virtual V_{dd}), 498.3 µV (virtual GND) and 237.4 mV (floating V_{dd}), 80.04 mV (floating GND) respectively.

The leakage current depends on the input states [10]. The experimental results in Table 1 shows the leakage current for different input states, where during the active mode (sleep signal is low) the leakage current is in range of pA while during the standby mode (sleep signal is high) the leakage current in range of nA leading to higher static power consumption.

From the simulation result, it is illustrated in Table 2 that the power consumption has been decreased during the standby mode due to eliminating the leakage current while the device is in the standby mode (the majority of the time) so the total power consumption is decreased which is reflected in the battery life time. The experimental results show for the DFF at

30 KHz with 30 % activity, 250 mV power supply that the maximum power consumption during the active mode is 8.565 nW and 1.625 nW during the standby mode as shown in Table 2, where all currents drawn from the supply were taken in account compared to previous work [6] in which they did not take the effect of the Idriver current in the simulation of the flip flop.

Table 1 Leakage current

Sleep		INPUT	Leakage Current
Active mode	0	0	629.8 pA
	0	1	968.3 pA
Standby mode	1	0	3.99 nA
	1	1	27.85 nA

Fig.11 illustrates the output waveform of the 10-bit shift register which operates at 30 KHz clock frequency with 30 % activity, 250 mV power supply where the maximum power consumption during the active mode is 37.25 nW, 11.85 nW during the standby mode and power delay product of 97.32 fJ.

Fig.12 shows the simulated output waveform of the 10-bit shift register which operates at 250 mV voltage source, 5 MHz clock frequency with 10% activity. The average power consumption is 6.429 nW while the maximum power in the active and sleep mode respectively are 45 nW and 22.5 nW and the PDP is 24.38 aJ.

The presented design is working properly at high frequencies. Fig.13 shows the output waveform of the ten bit shift register at 20 Mhz clock frequency with 50% where the voltage supply is 250 mV.

Table 2 Dynamic and Static power consumption

	Dynamic power (during active mode) (nW)	Static power (during standby mode) (nW)
Latch	8.565	1.625
One-bit shift register(30KHz)	37.25	11.85
Ten-bit shift register(5MHz)	45	22.5

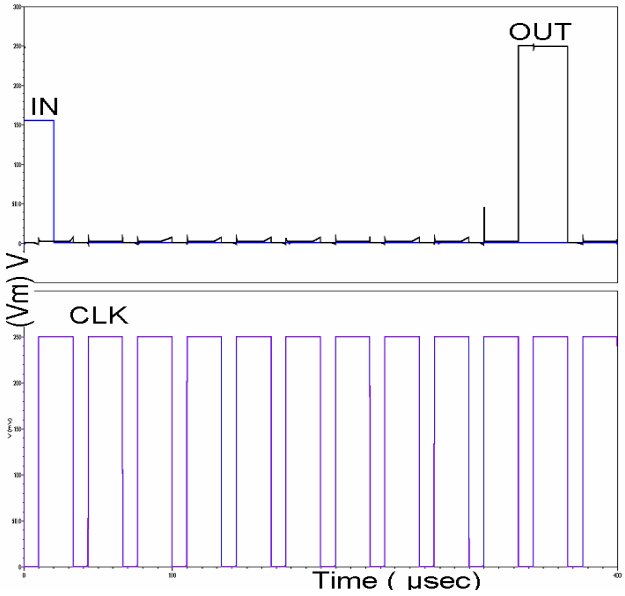

Fig.11 waveform of 10-bit Shift Register at 30 KHz clock frequency and 30% activity

The power consumption decreases as the activity decreases as illustrated in Fig.14. That is why this technique is very useful for the circuits, which spend the majority of the time in the standby mode awaiting a certain input.

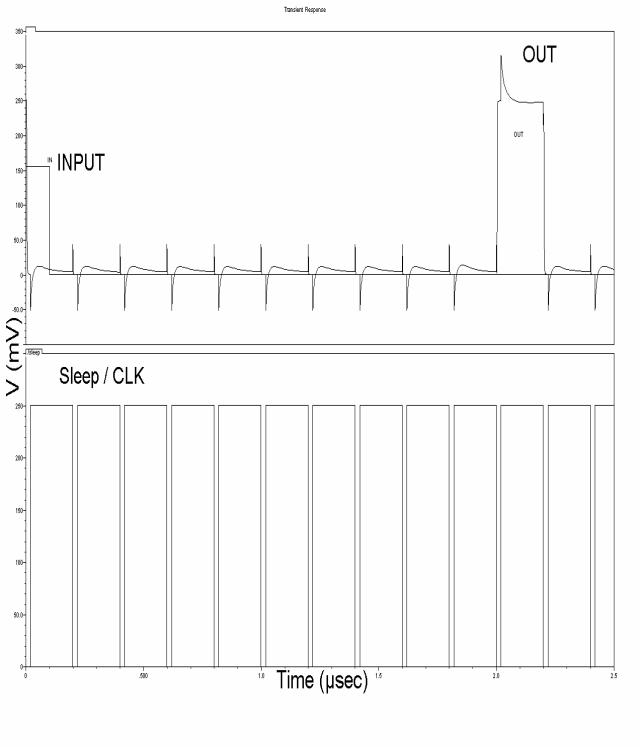

Fig.12 waveform of 10-bit Shift Register at 5 MHz clock frequency and 10% activity

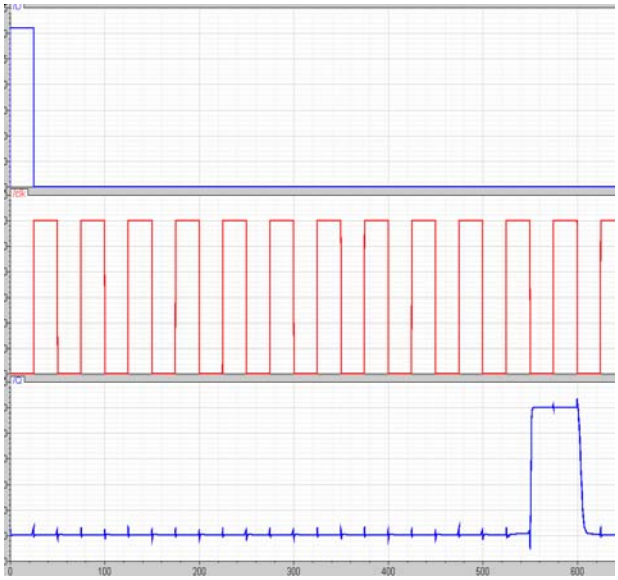

Fig.13 waveform of 10-bit Shift Register at 30 KHz clock frequency and 30% activity

VI. CONCLUSION

This journal illustrates the design of the low-power static latch in the sub-threshold region based on the MTCMOS technique to achieve high performance during the active mode and low power consumption by eliminating the possible leakage paths through combining the high and low threshold to prevent the leakage current during the standby mode. The low power static latch could be implemented in the SAR, reducing the power of this part which could benefit the entire wireless sensor. Finally, the journal proposed this latch to achieve 250mV supply voltage low power and high speed ten-bit shift register design using the 90nm technology, where the analysis and simulation confirmed the design of 10-bit shift register with 250mV at 5MHz for high speed applications and at 30KHz for low speed applications.

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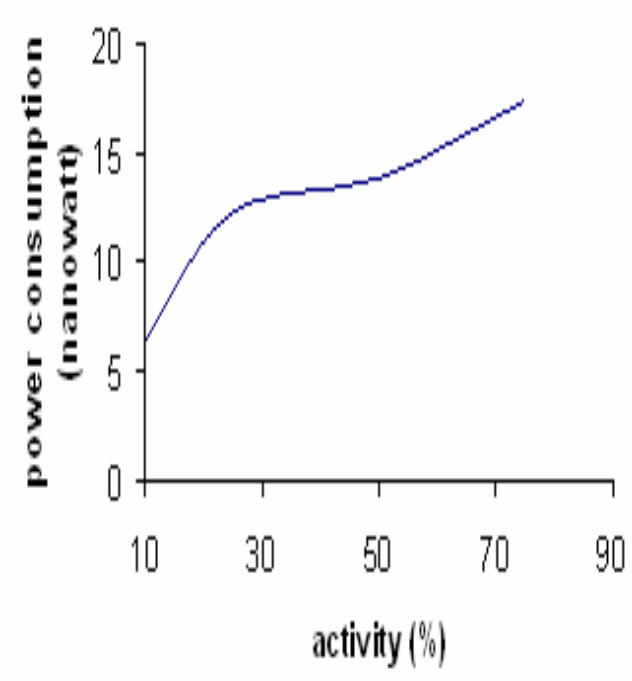

FIG.14 POWER CONSUMPTION VERSUS CIRCUIT ACTIVITY FOR 10-BIT SHIFT REGISTER.

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