The Design of High Frequency True Single Phase Clocking Divider-by-3 Circuit

Masayuki Ikebe, Yusuke Takada, Masaki Ohuchi, Junichi Motohisa and Eiichi Sano

***Abstract*— We evaluated the use of a true single phase clocking (TSPC) circuit as a high-frequency divider-by-3 circuit. This divider consists of two TSPC D-flip-flops (D-FFs) with NOR gate logic circuitry. To achieve high-speed operations as well as downsize the circuit, the NOR functions are implemented into the TSPC D-FF. We designed the divider using a 0.18-μm RF CMOS process; the circuit is 100 $\times$ 200 μm^2. Compared with the existing design such as a source coupled logic circuit, a 50% reduction of circuit area was achieved. The power consumption and operating frequency of the proposed divider was investigated. In the measurements, we confirmed the frequency divided by 3 at less than 3.14 GHz clock with 2.34 mW. The circuit is implemented in low-power high-frequency dividers for wireless local area network applications.**

***Index Terms*— SCL, TSPC, High frequency divider, Divider-by-3 circuit, High speed operation.**

I. INTRODUCTION

THE field of broadband communications has been rapidly expanding as the information society continues to grow. Relatively large amounts of data can now be handled with ease, and the exchange of image and music data is commonplace. In both wired and wireless communications, synchronous technology is indispensable, and this technology is used on various levels, such as the protocol and circuit levels. A divider generates a fraction of the reference frequency, and is used for a clock generator, a frequency synthesizer, and other operations [1], [2], [3].

An ordinary high frequency divider in a CMOS process consists of source coupled logic- (SCL-)[4] D-flipflops (D-FFs). Since the SCL uses a differential operation, this circuit can perform high-speed operations at low amplitudes (Fig. 1). The SCL circuit has two- cross coupled nMOSFETs, load pMOSFETs, differential-connection nMOSFETs and switching current sources.

When clk signal ϕ is logical "1", the SCL circuit works as a differential amplifier. The differential input is amplified and outputted. When clk signal ϕ changes from "1" to "0", the SCL circuit holds data by cross coupled nMOSFETs. In this way, the SCL circuit performs a D-latch operation which repeats "Data-thorough" and "Data hold" alternately.

However, for a divider-by-2 circuit, because a D-FF is required[5], [6], two SCL circuits which performs the D-latch operation are needed. Moreover, the circuit configuration of the divider-by-3 circuit needs two D-FFs and additional logic circuits. Therefore, it has been difficult to produce a high frequency divider with a small circuit composition.

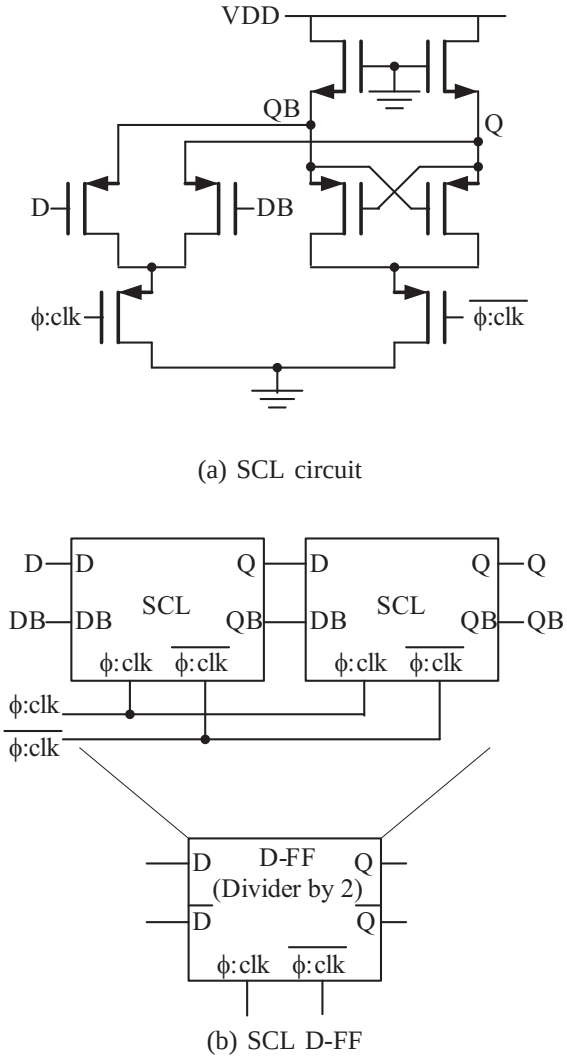

Fig. 1. Source-coupled logic circuit.

To overcome this problem, we propose new circuitry for high frequency division by 3 that has a TSPC architecture that can be used for various applications.

The remainder of this paper is organized as follows. In Section II, we describe the TSPC D-FF circuit and actual circuit design of divider by 3; in Section III, we present simulation results obtained using the proposed circuit, describe the layout design and discuss size of circuit area; and in

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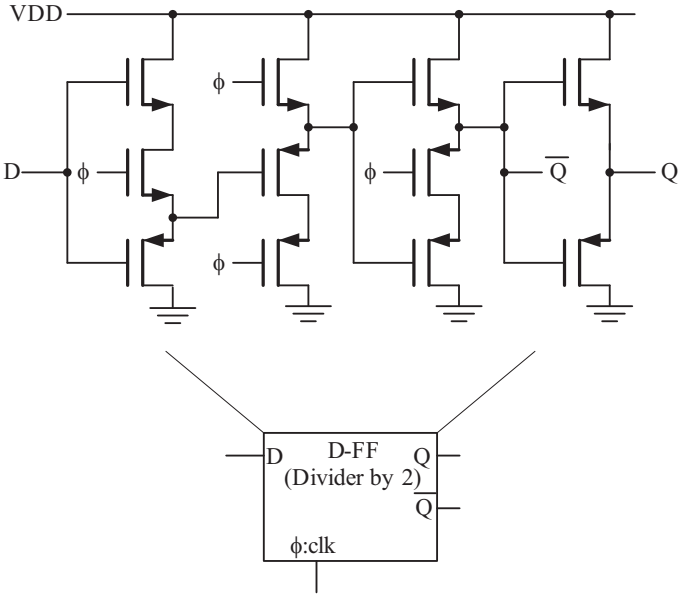


Fig. 2. True-single-phase-clocking circuit.

Section IV, we present measurement result.

II. TRUE SINGLE PHASE CLOCKING DIVIDER

A. Operation of TSPC logic circuit

A TSPC logic circuit alternately generates " Data-fetching state " and " Hold state " operations by switching between CMOS devices (in Fig. 2). Like a dynamic logic circuit that alternately performs " Pre-charge " and " Evaluate " operations in parasitic capacitance, the TSPC circuit operates a data fetch by using the pre-charge and data hold performed by the high impedance switching at the clock-signal timing[7], [8], [9], [10], [11], [12].

Figure 3 shows the D-FF operation of a TSPC circuit. When $\phi = L$, the first stage of the circuit runs as an inverter and outputs next state $\overline{Data[t+1]}$ as the input of the second stage. Because the bottom nMOSFET of the second stage turns off, the output of the second stage is always logical "1". Therefore the n- and p-MOSFET in the output part simultaneously turn off, and $\overline{Data[t]}$ is held in the parasitic capacitance of the third stage output line.

When $\phi \rightarrow H$, the state of $Data[t+1]$ is determined and then the circuit outputs it. At that time, if $Data[t+1] = 1$ and the input changes to $Data[t+2] = 0$, because the middle pMOSFET of the first stage turns off, the output data "$\overline{Data[t+1]} = 0$" doesn't change. If the $Data[t+1] = 0$ and the input changes to $Data[t+2] = 1$, the first stage output changes from $\overline{Data[t+1]} = 1$ to $\overline{Date[t+2]} = 0$. However, when $\phi \rightarrow H$, the parasitic capacitance of the second stage output is discharged. In this case, although the second stage input changes, the second stage output doesn't change. Therefore the third stage output also doesn 't change. In this way, the TSPC circuit performs the D-FF operation.

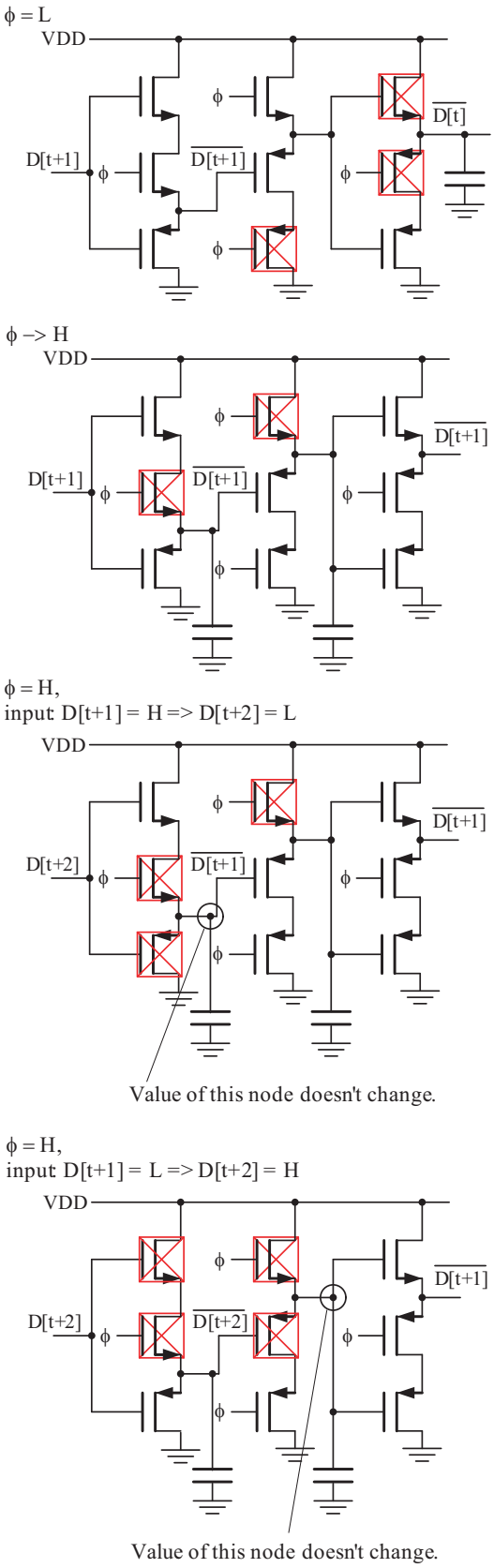


Fig. 3. D-FF operation of TSPC circuit.

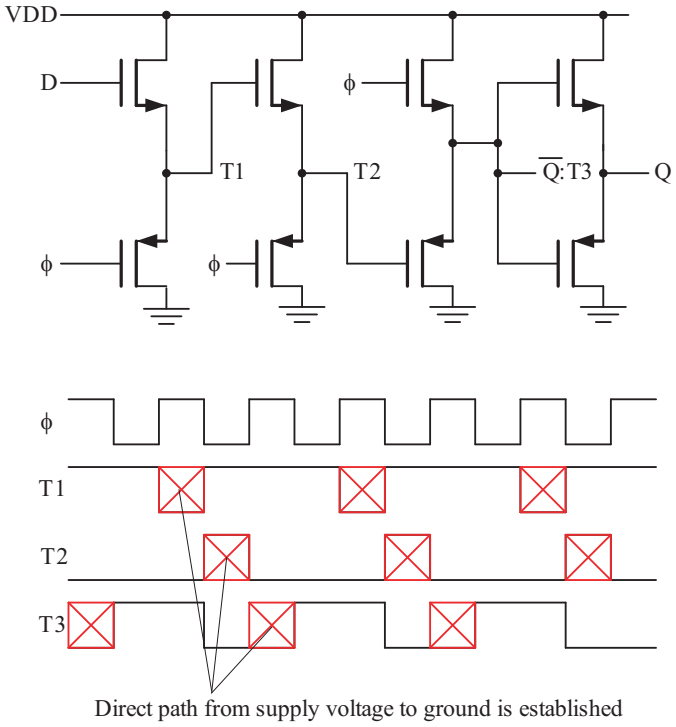


Fig. 4. Extended TSPC circuit and dividing-by-2 operation.

B. Extended TSPC logic circuit

The TSPC DFF is useful divide-by-2 unit in the high-speed frequency divider design. However, to increase the operating frequency, an extended-TSPC (E-TSPC) DFF was proposed[13], [14], [15]. Figure 4 shows the circuitry of an E-TSPC DFF and timing chart of dividing-by-2 operation, respectively. The E-TSPC logic circuit also alternately generates " Data-fetching state " and " Hold state " operations by switching MOSFETs. It operates a data fetch by using the pre-charge and data hold performed by the high impedance switching at the clock-signal timing, too.

Performing the D-FF function by the E-TSPC circuit, the output of the third stage is inverted. The D-FF operation is shown in Fig. 5. When ϕ = L, the nMOSFETs in the first- and the second stages simultaneously turn off. If the $Data[t]$ = "1", the pMOSFET of the first stage also turns off, the both MOSFETs of the first stage make the high-impedance condition at the output node, and $\overline{Data[t]}$ is held in the parasitic capacitance of the first stage-output line. Therefore the pMOSFET of the second stage turns on and the output node is precharged, and the output of the third stage doesn't change. At that time, if the input changes to $Data[t+1] = 0$, because the pMOSFET of the second stage turns off and the second stage output is already precharged, the second- and the third stage output data "$\overline{Data[t]} = 0$ and $Data[t] = 1$ " doesn't change.

If the $Data[t]$ = "0", the pMOSFET of the first stage turns on, the first stage output is precharged. The both MOSFETs of the second stage make the high-impedance condition at the output node, and $Data[t]$ is also held in the parasitic

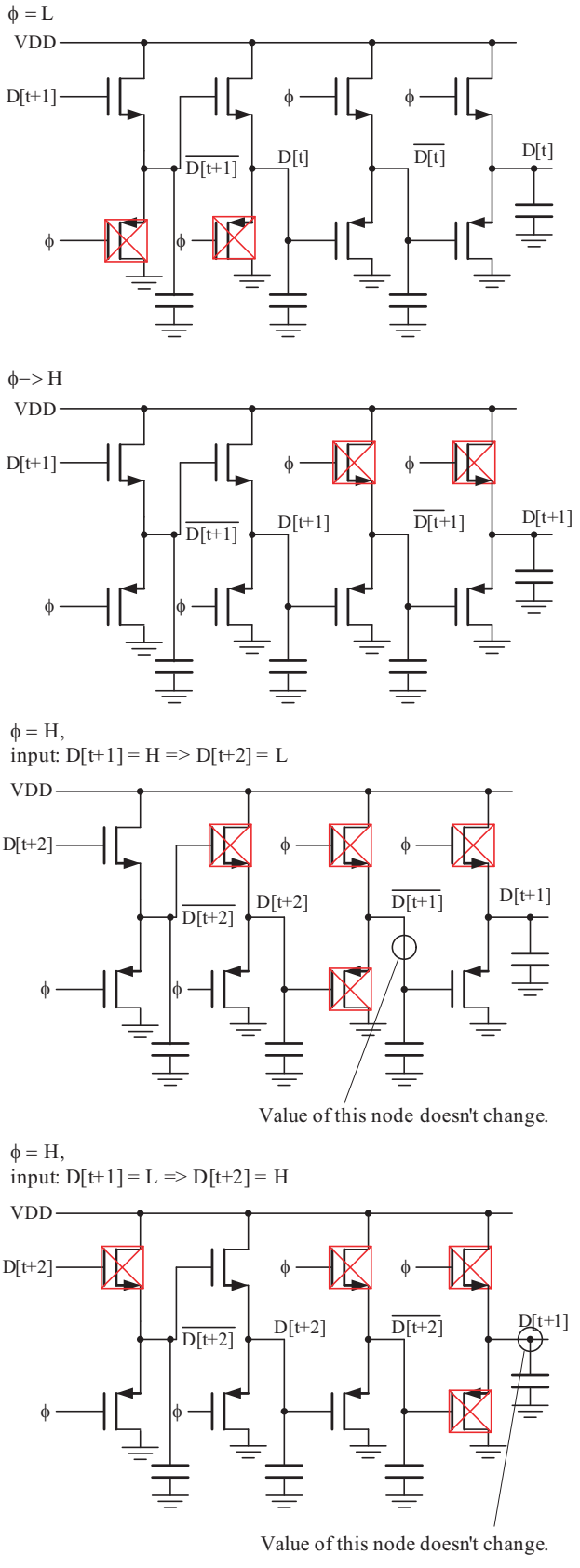
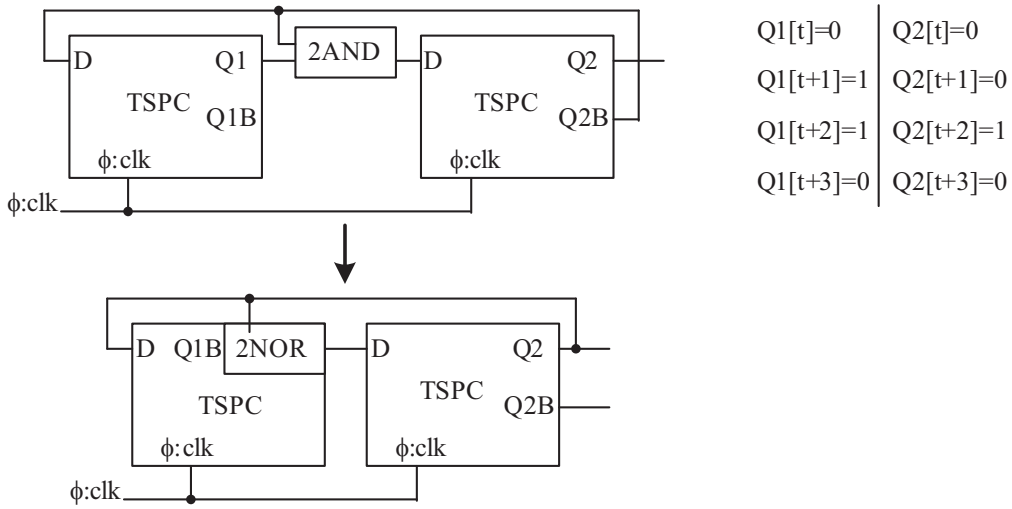
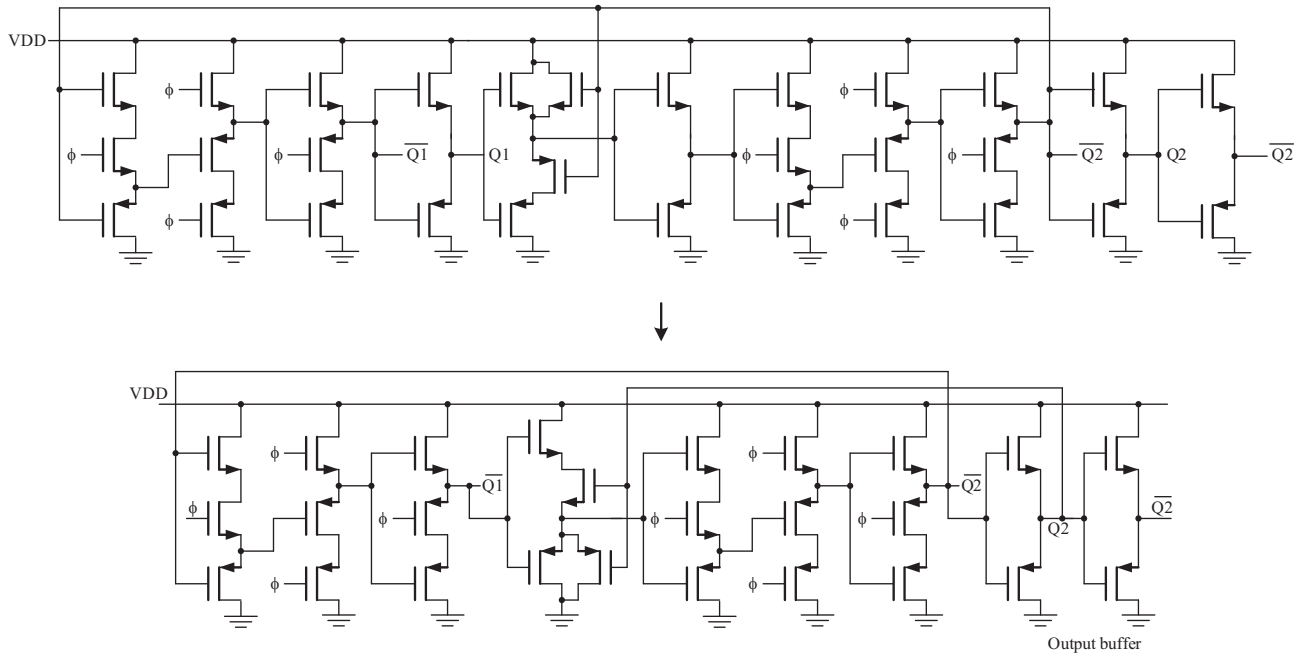


Fig. 5. D-FF operation of E-TSPC circuit.



(a) TSPC-divider-by-3 circuitry



(b) Actual TSPC-divider-by-3 circuit

Fig. 6. TSPC-divider-by-3 circuit.

capacitance of the second stage-output line. Therefore the output of the third stage also doesn't change. At that time, if the input changes to $Data[t+1]=1$, because the pMOSFET of the first stage turns off and the first stage output is already precharged, the second- and the third stage output data "$\overline{Data[t]}=1$ and $Data[t]=0$ " doesn't change.

When $\phi \rightarrow H$, the first stage of the circuit runs as a quasi pMOSFET-logic inverter and outputs current state $\overline{Data[t+1]}$ as the input of the second stage. The second stage of the circuit also runs as a quasi pMOSFET-logic one. Because the pMOSFET of the third stage turns off, output of the third stage is evaluated by the second stage output.

At that time, if $Data[t+1]=1$ and the input changes to $Data[t+2]=0$, because the nMOSFET of the third stage turns off, the output data "$\overline{Data[t+1]}=0$" doesn't change. If the $Data[t+1]=0$ and the input changes to $Data[t+2]=1$, the third stage output changes from $\overline{Data[t+1]}=1$ to $\overline{Date[t+2]}=0$. However, when $\phi \rightarrow H$, the parasitic capacitance of the final stage output is discharged. In this case, although the third stage input changes, the final stage output doesn't change. In this way, the E-TSPC circuit performs the D-FF operation.

The propagation delay of the E-TSPC unit is smaller than that of the TSPC unit because of the reduction of load capacitance. However, according to the timing chart of the E-TSPC circuit (in Fig. 4), all stage of the circuit runs as quasi

pMOSFET- and nMOSFET logic inverters, respectively.

When the circuit performs the D-FF function, because of the above inverter operations, there is a period during which a direct path from supply voltage to ground is established. The crossed areas in Fig. 4 mark the transition during which the short circuit takes place. The short current of the E-TSPC circuit is larger than the driving current of the TSPC one. Therefore it has been reported that the TSPC circuit had an advantage in the total power dissipation[16], [17], [18], [19].

C. TSPC divider-by-3 circuit

The proposed divider-by-3 circuit consists of sequential circuits based on the TSPC D-FFs and 2-AND gate logic. Figure 6 shows the proposed circuit and its truth table.

This circuit achieves frequency division by using logic operations. By AND logic, when only $Q1[t] = 1$ and $Q2[t] = 0$, $Q2[t+1]$ becomes "1". In other condition, $Q2$ becomes "0". The sequence of the truth table is performed repeatedly at each clock cycle. Therefore the circuit as shown in Fig. 3 performs frequency dividing by 3.

However this circuit is not suitable for high frequency uses. In the circuit configuration, the cascade connection between the D-FF and the AND gate degrades the frequency characteristic by adding additional delay to the circuitry[20], [21]. Therefore the technique of improving the high frequency characteristic is required. Here, using De Morgan's law, the binary logic of the connection can be transformed as follow equation.

$$Q_1 \cdot \overline{Q_2} = \overline{\overline{Q_1 \cdot \overline{Q_2}}} = \overline{\overline{Q_1} + Q_2} \qquad (1)$$

The NOR logic can be obtained from the AND one, and input of the logic function changed from $D[t+1]$ to $\overline{D[t+1]}$. Thus, we implemented the NOR function into the TSPC D-FF without using the optional AND gate circuit and reduced additional delay to the whole circuitry.

Because of the high-impedance condition, the third stage output of the TSPC circuit cannot be used for a differential output. The differential output is achieved by using an additional inverter. The inverter also optimizes duty of the output signal.

III. CIRCUIT DESIGN AND ITS SIMULATION

We designed the divider by using a 0.18-μm mixed signal/RF CMOS process with one poly and six metal layers. In this design, the output-impedance matching was not set to 50 Ω terminated, because we assume that the next stage circuit is a conventional logic circuit that has a high input impedance. The ratio of the size of the p- and n-MOSFET was set to 3:1 due to the mobility of the MOSFETs, but the actual sizes were determined by the operating frequency. By the MOSFETs size of the additional output inverter, we control the signal duty.

Figure 7 shows the size depending on the operating frequency. The power dissipation for a 3-GHz operation was 2.7 mW under typical conditions. The 4 GHz operation can be achieved over the scale factor "2". The operating frequency also increased as the MOSFET size became large, but over

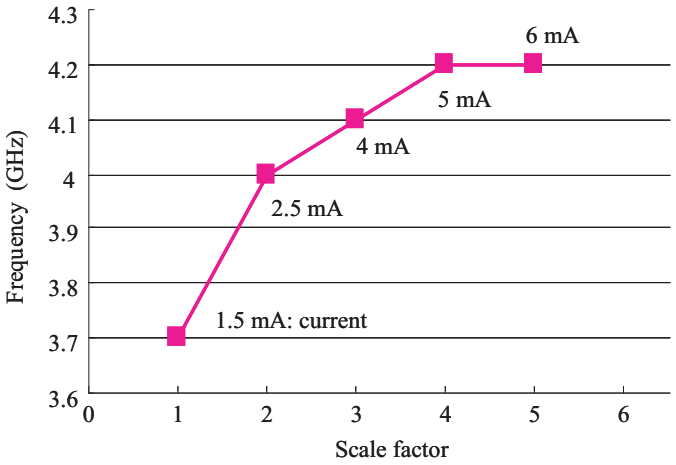


Fig. 7. Operating frequency vs. MOSFET size for current dissipation of proposed divider.

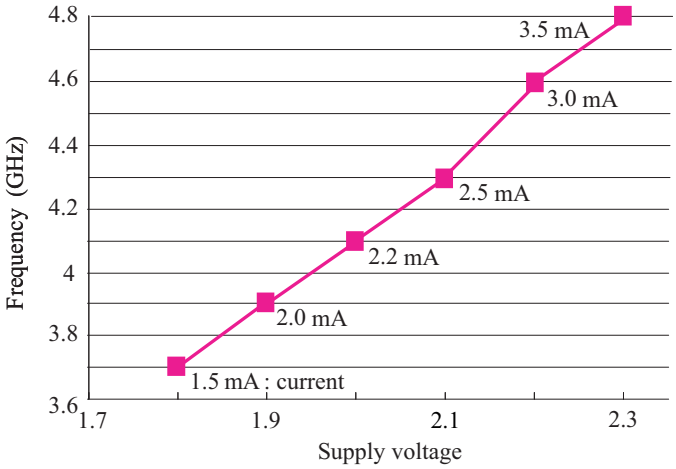


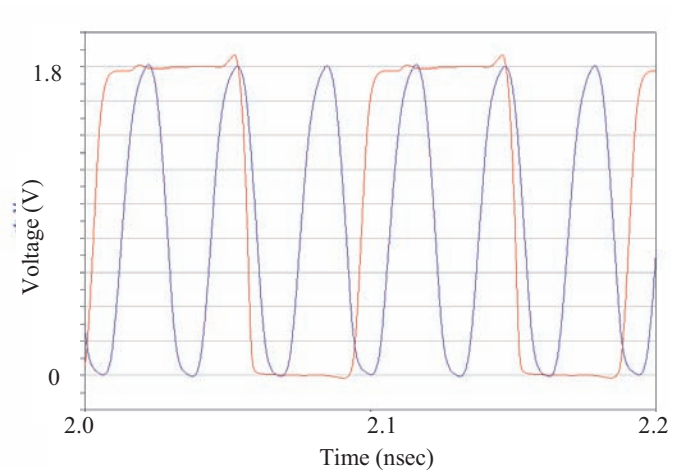
Fig. 8. Operating frequency vs. supply voltage for current dissipation of proposed divider.

the scale factor "5" it was saturated. The main reason for this saturation is the load capacitance of the circuit. The load capacitance depends on the MOSFET size. Therefore, although the driving power increases, the propagation delay also becomes large and the operating frequency is saturated.

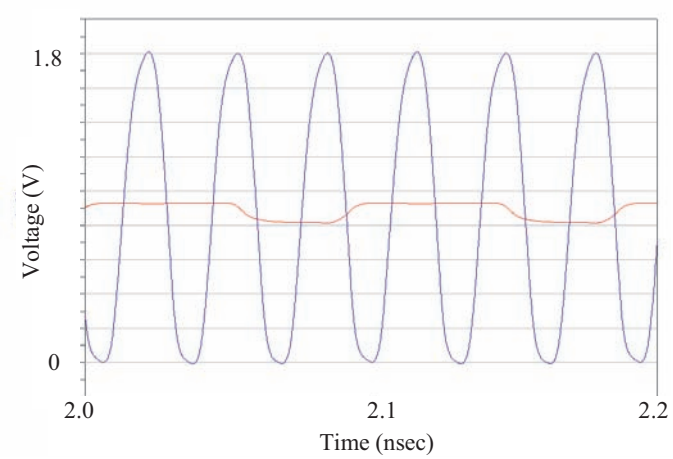
Figure 8 shows the supply voltage depending on the operating frequency. In this simulation, the load capacitance doesn't change. Therefore the operation frequency increased as the supply voltage increased. The 4.8 GHz operation can be achieved at the supply voltage 2.3 V.

The result of transition simulation is shown in Fig. 9. We confirmed that the circuit could convert the frequency from 3 GHz into 1 GHz. Based on the measurement setup, we also include the result for 50 Ω terminated configuration. Although the output amplitude was small, we were able to confirm division operations up to 3.6 GHz using our design by conducting circuit simulations under typical conditions.

Figure 10 and 11 shows the layout of the circuit and the SCL-divider-by-2 circuit. The SCL divider was designed for 3 GHz operation. Both of circuit sizes were almost the same. When compared to a standard SCL configuration, because the SCL-divider-by-2 circuit included one D-FF circuit, we



(a) Open



(b) 50 Ω terminated.

Fig. 9. Transition simulation results.

decreased the circuit area by 50% using the SCL D-FF basis. Our circuit was 100 × 120 μm^2. Figure 12 shows the chip micrograph of our circuit.

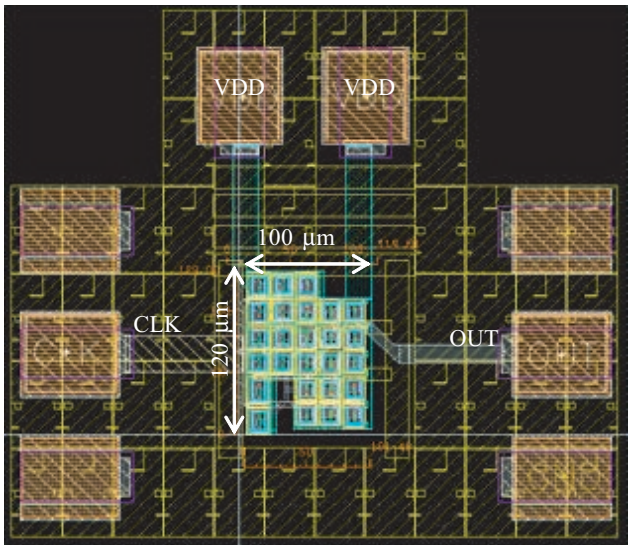


Fig. 10. Layout of proposed divider by 3.

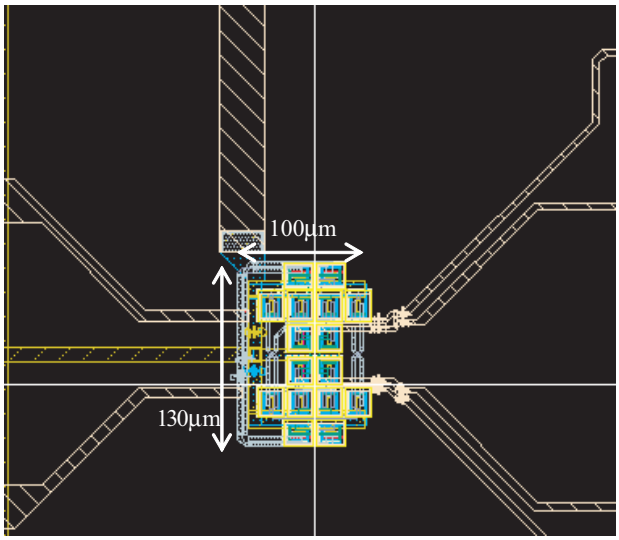


Fig. 11. Layout of SCL divider by 2.

IV. MESUREMENT RESULT

Figure 13 shows the measurement setup. One of the fabricated chips was placed on a probe station. The transition characteristic and the frequency characteristic were measured with an oscilloscope and a spectrum analyzer. The signal generator port was connected to the divider input. The bias voltage $VDD/2$ was given to the divider thorough a Bias-T.

In this measurement, an input signal with 7 dBm was applied to the divider through a cable with 50 -Ω characteristic-impedance configuration. The measured results are shown in Fig. 14, 15, 16 and 17. We confirmed the operation of dividing by 3 at less than 3.14 GHz with 2.34 mW. Moreover, when supply voltage VDD = 2.3 V was given, operation frequency increased up to 4 GHz with 4.78 mW.

Since the measurement setup was a 50 -Ω termination, the output amplitude was small. This result was same as that in simulation one. However, during the measurement, when an input signal of more than 3.14 GHz was given to the circuit, it worked as a divider by 4. The main reason for this unusual operation is the parasitic capacitance of the feedback line. If a signal delay occurs, the updating of the next stage also falls behind.

V. APPLICATION EXAMPLES

The following are a few applications of the high-frequency divider by 3 circuits. A prescaler of a phase locked loop (PLL)[22] is stated as the first application. For the programmable prescaler, a switching controller between the dividing by 2 and 3 is required. In our method, implementing logic function, it is easy to achieve the above circuit configuration (in Fig. 18).

Next, a frequency synthesizer for MB-OFDM UWB system is stated as the application of our circuit[23]. Band group

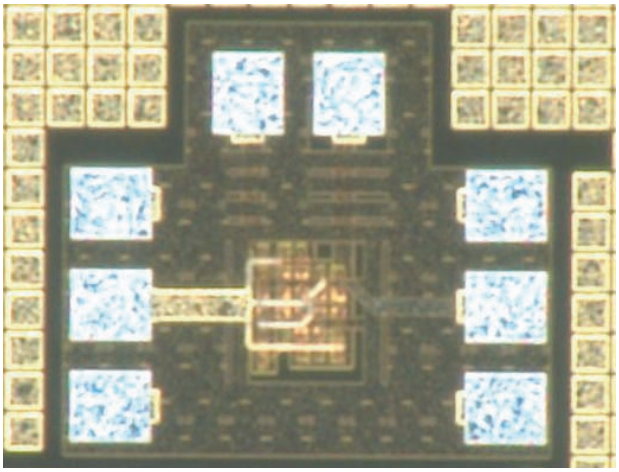


Fig. 12. Chip micrograph of proposed divider by 3.

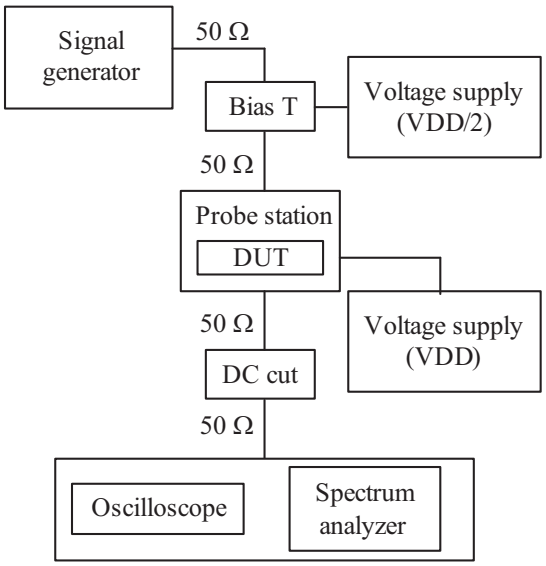


Fig. 13. Measurement setup.

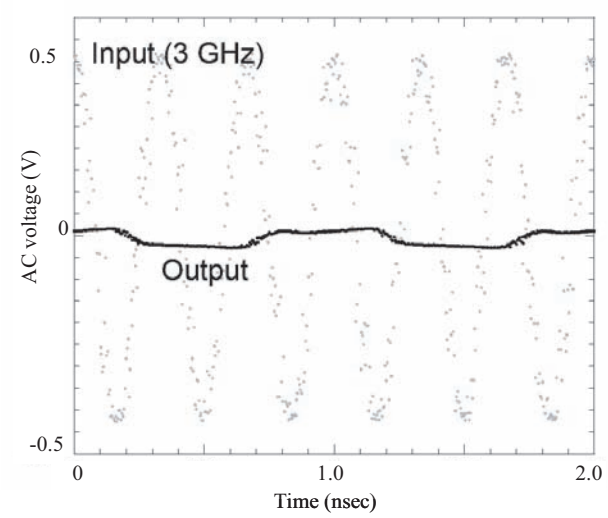


Fig. 14. Measurement results of proposed circuit.

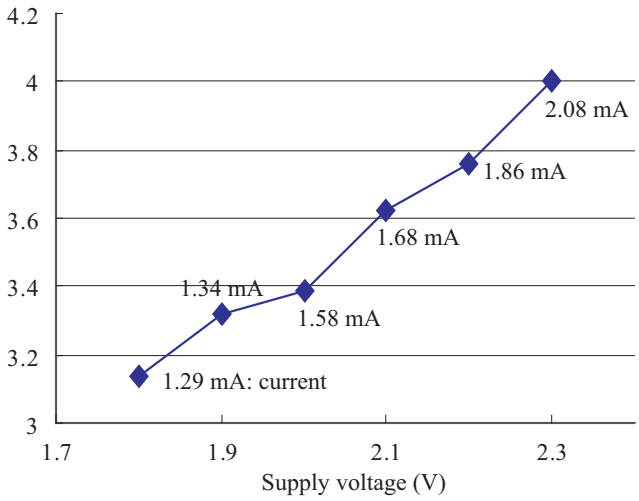


Fig. 15. Maximum Operating frequency vs. supply voltage for current dissipation.

allocation for MB-OFDM band plan from 3.1 GHz to 10.6GHz is shown in Fig. 19. In MB-OFDM system, 14 frequencies synthesis by a few oscillators is required. Therefore the frequency dividing operation is very important. The bandwidth of each band of MB-OFDM system is 528 MHz. The OFDM modulation consists of 128 sub channels with 4.125 MHz. For reduction of propagation degradation by multi-path problem, fast frequency hopping is performed in a band group (ex. band“1” → band“2” → band“3” → band“1”). With LSI process development, the MB-OFDM system has shifted to composition applicable also to the band group 1 of mandatory and other band groups of high frequency.

Covering all frequencies of the MB-OFDM, we consider that synthesis of center frequency in band groups from a 10.296 GHz oscillator[24] and a 6.336 GHz one. According to the group 1: 3.960 GHz, it can be obtained by difference-frequency mixing the base frequency 10.296 GHz and the temporal frequency 6,336GHz through LPF. About the group 3 and 4, by the dividing by 2 and 4, the other temporal frequencies 3.168 GHz and 1.584 GHz are synthesized from the frequency 6.336 GHz. Obtained two frequencies are mixed with 10.296 GHz for generating the center frequencies of the band group 7.128 GHz and 8.172 GHz through LPF. Upper side band of obtained frequency from 10.296 GHz and 6.336 GHz is more than 10 GHz. Therefore demand for the LPF is moderated.

Here, considering synthesis of subband in each band group, because the subband frequency 0.528 GHz is required, this frequency is obtained from the temporal frequency 3.168 GHz by dividing-by-6 function. At that time, the dividing-by-3 circuit is important for above operation. Using the frequency 0.528 GHz, all subband can be synthesized from center frequencies in each band group. In this way, the multi-frequencies of MB-OFDM system are obtained by mixers, oscillators, and

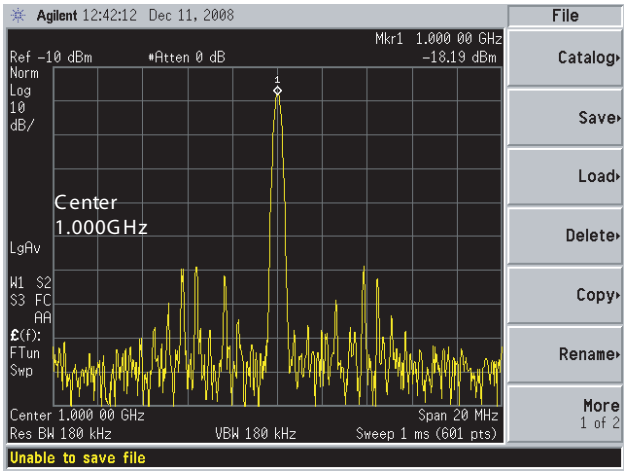


Fig. 16. Power spectrum of 3 GHz conversion.

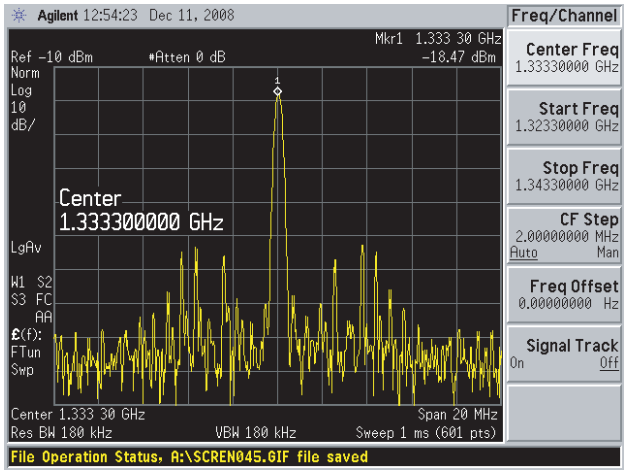


Fig. 17. Power spectrum of 4 GHz conversion.

dividers.

VI. CONCLUSION

We designed a high-frequency-TSPC divider-by-3 circuit. This divider, which has two TSPC D-FFs, converted a 3-GHz reference signal into a 1 GHz one with only a 2.7 mW. The circuit was 100 $\times$ 120 μm^2 and was constructed using a 0.18-μm mixed signal/RF CMOS process. We fabricated and measured the designed divider. A 3-GHz operation of dividing by 3 with 2.34 mW was confirmed by measurement.

ACKNOWLEDGMENT

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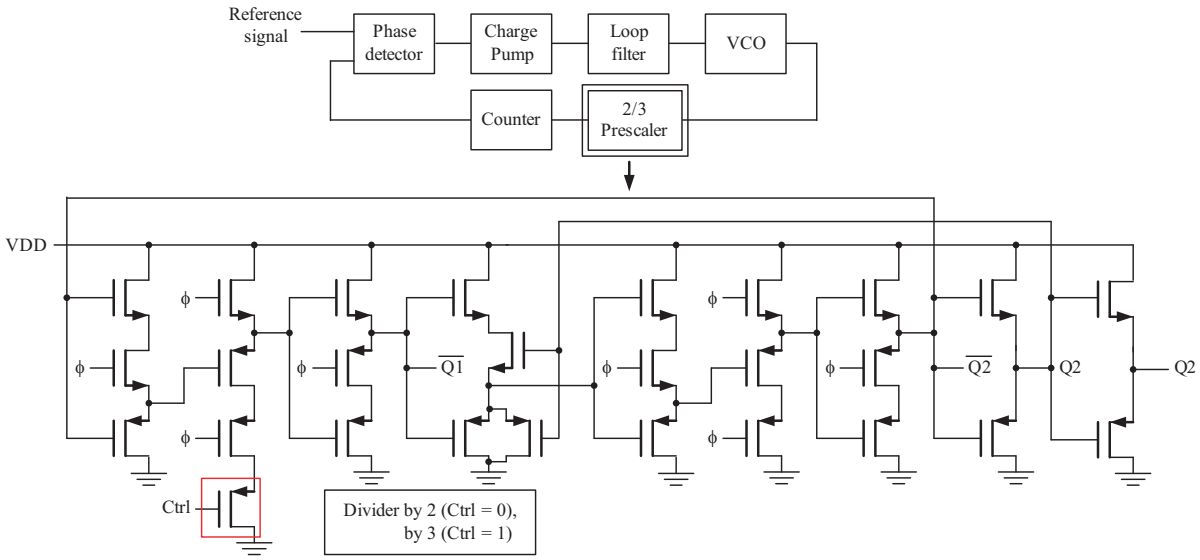

Fig. 18. Prescaler of PLL.

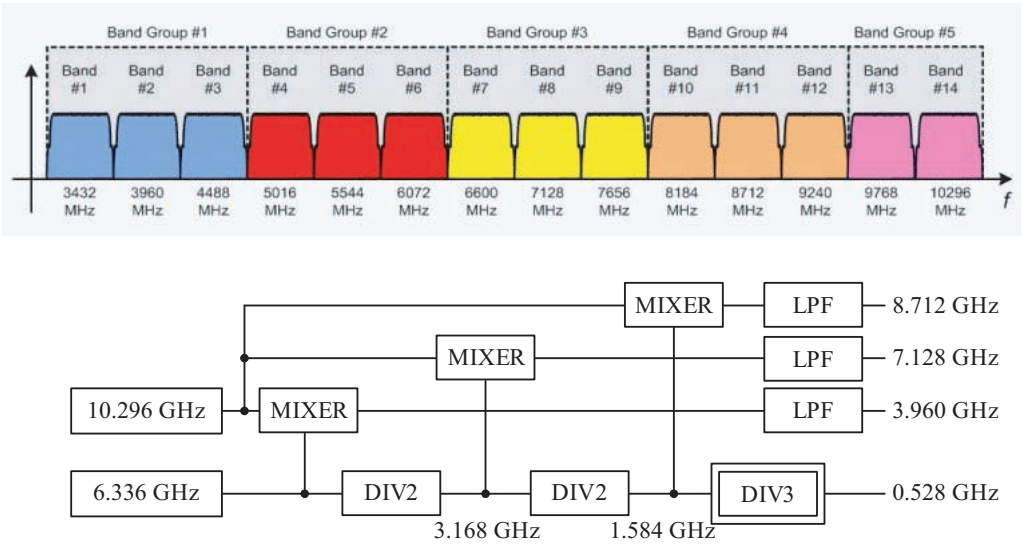

Fig. 19. Band allocation and frequency synthesizer of MB-OFDM.

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