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Linearization of Doherty amplifier with second harmonics and fourth-order nonlinear signals

Nataša Maleš Ilić, Aleksandar Atanasković, Bratislav Milovanović

***Abstract*—**In this paper, influence of the second harmonics and fourth-order nonlinear signals on the efficiency and linearity of three-stage Doherty amplifier loaded with harmonic control circuits is analyzed. Amplifier is designed with LDMOSFETs in carrier and peaking amplifiers with the same periphery and in periphery relations 1:2.5:2.5. The signals for linearization are extracted at the output of peaking cells. The carrier and peaking amplifiers are loaded with the harmonic control circuit that provides the optimal impedance for the signals for linearization and either an open or short circuit for the third harmonics. Analysis of three-stage Doherty amplifier linearization with the approach where signals for linearization are adjusted in amplitude and phase and inserted at both carrier cell input and output have been performed in simulation by ADS. Afterwards, the linearization technique effects to Doherty amplifier have been proofed experimentally on a standard two-way Doherty amplifier. Measurements of the third- and fifth-order intermodulation product suppression in case when the signals for linearization are included into the amplifier input have been carried out.

***Keywords*—**Doherty amplifier; harmonic control circuit; fourth-order nonlinear signals; linearization; power-added-efficiency; second harmonics

I. INTRODUCTION

Current wireless communication systems transmit modulated signals very rapidly with high-peak-to-average ratio. Demanding requirements of new systems (CDMA2000, W-CDMA, OFDMT etc.) in order to meet both linearity and high power efficiency present a serious task for transmitter designers. The Doherty amplifier is capable of achieving the requirements of the power amplifiers in base station concerning a high efficiency. Various linearization methods of Doherty amplifier have been reported, which are post-distortion-compensation [1], the feedforward linearization technique [2], the predistortion linearization technique [3] and combination of those two linearization techniques [4].

The linearization effects of the fundamental signals' second harmonics (IM2) and fourth-order nonlinear signals (IM4) at frequencies that are close to the second harmonics to the standard (two-way, three-way and three-stage) Doherty amplifiers were investigated in [5] by applying the approach where signals for linearization, IM2 and IM4, are injected together with the fundamental signals into the carrier amplifier input and put at its output [6]. In papers [7] and [8], a standard two-way Doherty amplifier was extended to support class-F operation in order to achieve higher efficiency. Additionally, feedforward and digital feedback predistortion linearization techniques were implemented in [7] and [8], respectively, to improve the linearity. The linearization of standard three-stage Doherty amplifier, with LDMOSFETs in carrier and peaking amplifiers in periphery relations 1:2.5:2.5, was considered in paper [9]. In addition, three-stage Doherty amplifier was loaded with harmonic control circuit (HCC), which represents the optimal impedance for the second harmonics and open or short circuit for the third harmonics at the output of cells. These configurations denoted as HCC class-3F and class-3IF were presented in [10] and [11], respectively. When HCC represents an open circuit for the third harmonics at the output of carrier cell, whereas it shorts the third harmonics at the outputs of the peaking cells configuration was named HCC class-F-2IF and considered with the same transistor size [12] and with transistor size ratio 1:2.5:2.5 [13].

In this paper, three-stage Doherty amplifier named HCC class-IF-2F is analyzed. Amplifying cells are loaded with HCC that is the optimal impedance for the second harmonics and short circuit for the third harmonics at the carrier cell output and the open circuit at two peaking amplifier outputs. The signals for linearization are extracted at the output of peaking cells that are biased at various points to provide the appropriate power levels and phase relations of IM2 and IM4 signals. After been adjusted in amplitude and phase the signals from the output of one peaking amplifier are injected at the input of carrier amplifier, while ones appeared at the output of another peaking cell are put to the carrier amplifier output. All results obtained are compared to the class-F-2IF for cases with the same and various transistor peripheries. Moreover, frequency range of the linearization technique is extended by including tantalum capacitors at the input and output of transistors in amplifying cells [14]. Results are shown for HCC class F-2IF with the same periphery. All results have been achieved by using software Advance Design System-ADS.

On the top of that, the effects of linearization technique that utilizes second harmonics and fourth-order nonlinear signals have been verified experimentally on a standard two-way Doherty amplifier. The signals for linearization generated at the output of peaking cell are adjusted in amplitude and phase through the linearization branch. Measurements are performed for the case when signals for linearization are run at the carrier amplifier input.

Nataša Maleš-Ilić, Aleksandar Atanasković, and Bratislav Milovanović are with the Faculty of Electronic Engineering, University of Nis, Aleksandra Medvedeva 14, 18000 Nis, Serbia, phone:+38118529137

e-mails:[natasa.males.ilic;aleksandar.atanaskovic;bratislav.milovanovic]@elfak.ni.ac.rs

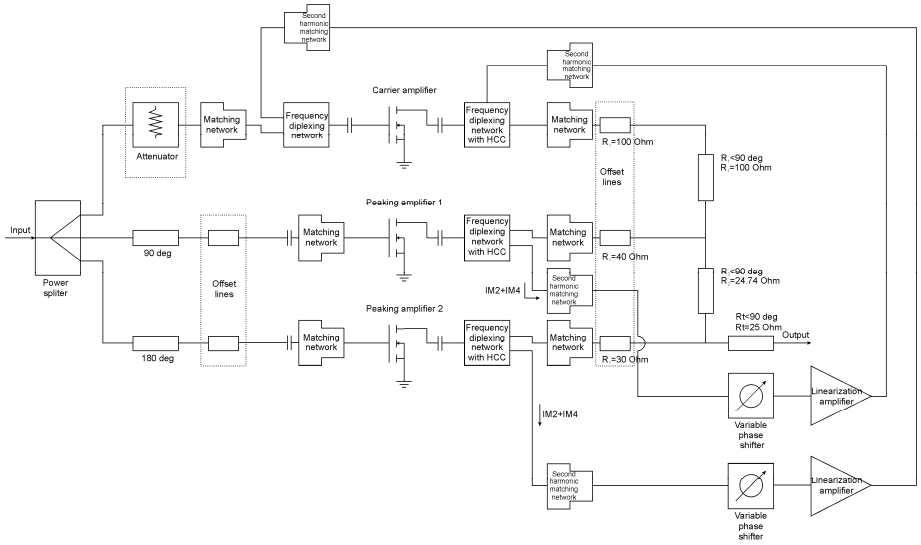


Fig.1 Three-stage Doherty amplifier with additional circuit for linearization

Section II and III includes the design of three-stage Doherty amplifier with harmonic control circuit and circuit for linearization. All results referring to the intermodulation products and efficiency obtained in simulation for two sinusoidal as well as digitally modulated signals by applying the linearization approach are included in section IV. A theory relating to the linearization approach applied to two-way Doherty amplifier in experiment is given in the section V. The realization process of two-way Doherty amplifier and additional linearization circuit is described in section VI. Measured results of linearization for two sinusoidal fundamental signals, i.e. output spectrum before and after linearization and results for the range of carrier output power-are included in this section, as well. The conclusions are reported in section VII.

II. THREE-STAGE DOHERTY AMPLIFIER DESIGN

The amplifier is designed in configuration with two quarter-wave impedance transformers in the output combining circuit [15], [16]. The output impedances of the amplifier cells are selected to satisfy the output power relations between the carrier and peaking cells. In addition, the transmission lines in the output combining circuit are practical for realization with not too high or too low characteristic impedances as shown in Fig. 1.

The amplifying cells are designed using Freescale's MRF281SR1 LDMOSFET with a 4-W peak envelope power level (PEP) according to the non-linear Motorola Electro-Thermal (MET) model included in ADS library. When periphery of transistors is in relations 1:2.5:2.5, Freescale's MRF282S LDMOSFET is utilized for the peaking cells (MET model exhibits a 10-W PEP level).

The matching impedances for source and load of amplifying cells at 2.14GHz are selected to satisfy the high efficiency. The input matching is performed for 50Ω, while the output matching is designed to transform the optimum output impedance of the carrier and two peaking cells to 100Ω, 40Ω and 30Ω, respectively.

The carrier cell is biased at class-AB with $V_G = 5.1\text{V}$ (13.5%I_{DSS}). Two peaking amplifiers operate in class-C. The drain bias voltage $V_D = 26\text{V}$ is the same for all cells.

Offset lines are incorporated at the output of peaking cells to minimize the effective loading of the peaking cells in state when those amplifiers do not operate (low-power range). In order to compensate for phase relation distortion in Doherty amplifier an appropriated offset line is adjusted at the output of carrier cell.

The peaking amplifiers are driven by signals with 1dB higher power than that of the carrier amplifier according to the analysis of uneven power drive performed in [17]. Maximum output power achieved by the Doherty configuration is 41dBm for configuration with the same transistors in amplifying cells and 44dBm for transistor periphery relations 1:2.5:2.5.

III. LINEARIZATION

Theoretical analysis of the linearization approach that uses the second harmonics and fourth-order nonlinear signals for linearization has been given in [5], [6], and [11]. According to this, it is possible to reduce spectral regrowth caused by the third-order distortion of fundamental signal (IM3) by choosing the appropriate amplitude and phase of IM2 signals injected at the input and output of the amplifier. Additionally, the fifth-order intermodulation products (IM5) can be suppressed by adjusting the amplitude and phase of IM4 signals that are injected at the input of amplifier and put at its output.

The IM2 and IM4 signals generated at the output of peaking amplifiers are extracted through HCC diplexer circuits. It separates the fundamental signals and signals for linearization that are matched to the impedance for optimal power level. Also, the frequency diplexer in configuration depicted in [5] is inserted at the carrier amplifier input with the independent matching circuits for the fundamental and signals for linearization.

Table I. Output spectrum of three-stage Doherty amplifier before and after the linearization for HCC class-IF-2IF and HCC class-F-2IF for two-tone test at frequencies 2.139GHz and 2.141GHz

Type	IM3 (dBm)			IM5 (dBm)			Fun. signals (dBm)		
HCC	Freq. (GHz)	Bef.	Aft.	Freq (GHz)	Bef.	Aft.	Freq. (GHz)	Bef.	Aft.
LDMOSFET size ratio 1:1:1, Input power 20dBm									
Class-IF-2F	2.137 2.143	16.14 16.06	-8.08 -3.36	2.135 2.145	5.22 6.40	-8.96 -14.98	2.139 2.141	32.92 33.00	32.51 32.89
Class-F-2IF	2.137 2.143	16.17 16.40	-0.10 -0.40	2.135 2.145	3.78 6.51	-4.49 -7.06	2.139 2.141	32.66 32.80	32.08 32.44
LDMOSFET size ratio 1:2.5:2.5, Input power 23dBm									
Class-IF-2F	2.137 2.143	21.78 23.01	6.25 7.14	2.135 2.145	2.74 10.21	-7.27 -6.26	2.139 2.141	36.71 36.59	36.11 36.41
Class-F-2IF	2.137 2.143	19.79 19.67	0.04 0.39	2.135 2.145	-1.80 11.78	-11.96 -9.76	2.139 2.141	36.96 36.94	36.23 36.27

This configuration provides the linearization of Doherty amplifier by the simultaneous injection of IM2 and IM4 signals at the input and output of the carrier amplifier. Those signals are generated at the output of peaking amplifiers that are biased at different points to produce adequate amplitude and phase relations between IM2 and IM4 signals. The IM2 and IM4 signals are tuned in amplitude and phase by the amplifier and phase shifter over two paths as given in Fig. 1.

Consequently, the carrier amplifier is harmonically controlled at input and output. This configuration enables higher gain of class-AB carrier amplifier with lower power of intermodulation products in reference to the standard class-F or class-IF amplifier biased at pinch-off [18].

IV. Simulation results

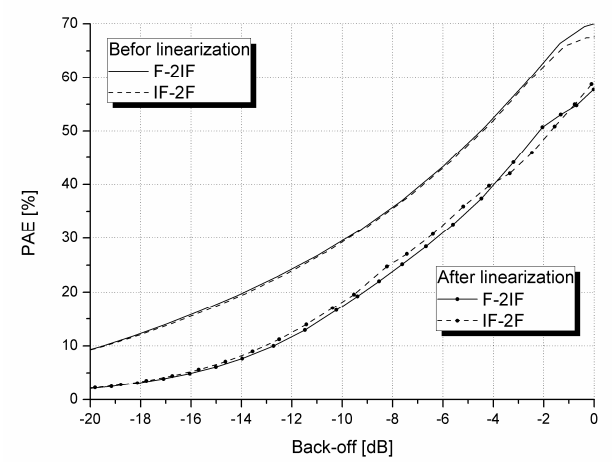
In this paper, three-stage Doherty amplifier in HCC class-IF-2F is analyzed by ADS program and compared to HCC class-F-2IF. The analysis carried out in both configurations include the optimization of offset line length in the carrier cell output in order to compensate for the time delay between amplifying cells when the influence of additional circuit for linearization is considered. The HCC class-F-2IF has been already analyzed in [12] and [13]. However, the length of offset line was not optimized with the addition of linearization circuits.

The linearization results for two-tone test at frequencies 2.139GHz and 2.141GHz achieved for designed three-stage Doherty configurations are given in Table I. It compares output spectra before and after the linearization in case of 20dBm (same transistors) and 23dBm (different transistor periphery) input power of fundamental signals. In the case of the same transistor periphery, we have achieved better linearity for class-IF-2F, whereas for different transistor periphery, class-F-2IF has slightly lower IM3 and IM5 products before linearization and also, few decibels better results of linearization are obtained. There is no significant degradation of the output fundamental signals in all cases.

Power-added-efficiency (PAE) for three-stage class-F-2IF and class-IF-2F Doherty amplifiers before and after the linearization is presented in Fig. 2. PAE before linearization relates to the case when amplifying cells are loaded for operation at standard class-F (short circuit for the second harmonics and open circuit for the third harmonics) or IF (open circuit for the second harmonics and short circuit for the third harmonics) in combinations denoted as F-2IF and IF-2F. A quiescent bias of carrier cell is 3.8V (pinch-off), a standard bias point for class-F and IF operation. In case of the same transistor periphery, PAE of class-F-2IF and class-IF-2F are 72% and 67%, respectively, at maximum power (0dB back-off), 44% at 6dB back-off (35dBm total output power) and 25% at 12dB back-off (29dBm total output power). Fig. 2 shows that PAE in case of the additional linearization circuit (carrier cell is now biased at 5.1V) drops in reference to the case of Doherty without linearization, so that it is 59% and 58% at maximum power, 33% and 31% at 6dB back-off and 13% and 12% for HCC class-IF-2F and class-F-2IF, respectively.

When transistor periphery is in 1:2.5:2.5 relations, PAE of class-F-2IF is 62% at maximum power (0dB back-off), 47% at 6dB back-off (38dBm total output power) and 33% at 12dB back-off (32dBm total output power). Under the same conditions, class-IF-2F exhibits 64%, 41% and 28% at the same back-off points. PAE in case of the additional linearization circuit for class-F-2IF falls by 4%, 14% and 17% and for class-IF-2F by 7%, 7% and 10% at back-off points in reference to the case without linearization. Also, Fig. 2 illustrates minor differences between PAE of class-F-2IF and class-IF-2F Doherty amplifiers after applying linearization. PAEs are almost equal at maximum power for two considered cases of transistor periphery. However, characteristic degrades

faster in the case of same transistors.



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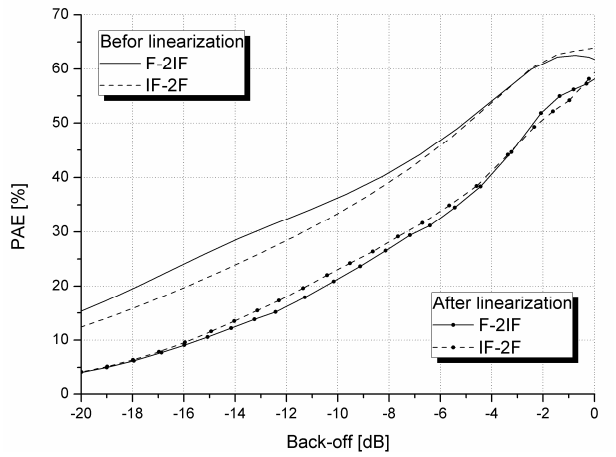
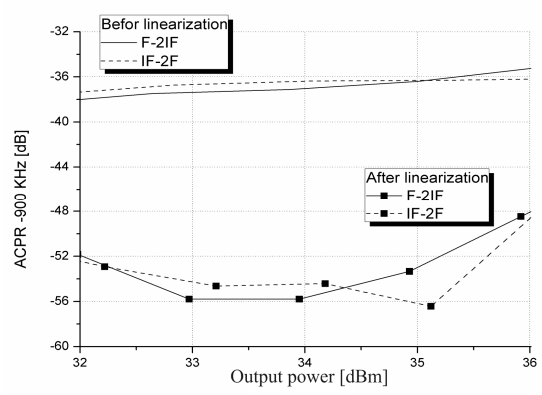


b)

Fig. 2 Power-added-efficiency of three-stage Doherty amplifier: a) same; b) different transistor periphery

Figures 3 and 4 show adjacent channel power ration as the effects of three-stage Doherty amplifier linearization (class-F-2IF and class-IF-2F) for CDMA digitally modulated signal with 1.25MHz spectrum width at ±900kHz and ±2100kHz offsets from carrier frequency 2.14GHz. The results have been accomplished for the average output power ranging from 32dBm to 36dBm for the same transistors and 35dBm to 40dBm in transistor periphery 1:2.5:2.5.



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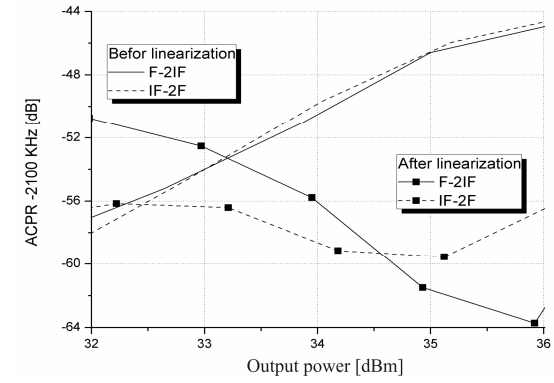

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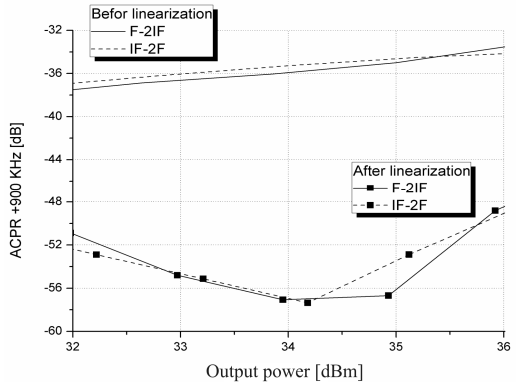

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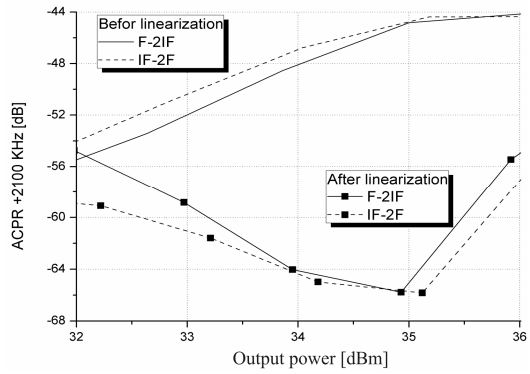
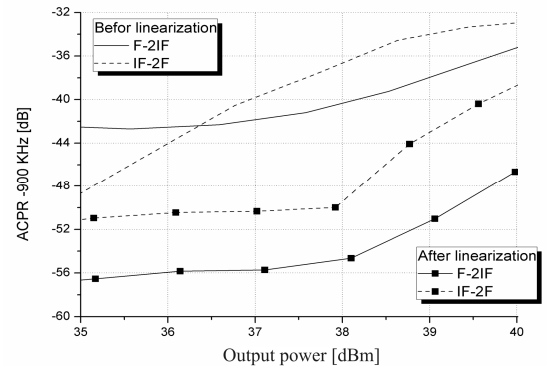


d)

Fig. 3 ACPR of HCC three-stage Doherty amplifier in a power range, before and after linearization, at offsets from carrier frequency: a) -900kHz; b)-2100kHz; c) +900kHz; and d) +2100kHz, in case of same periphery transistors



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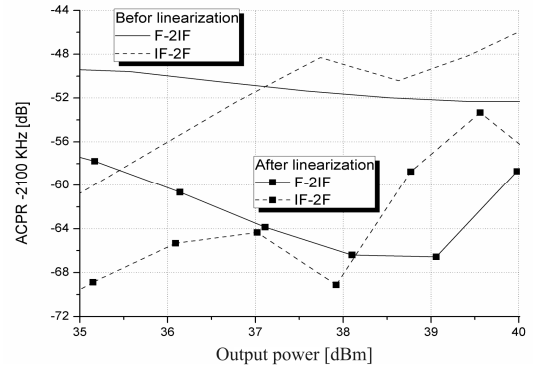

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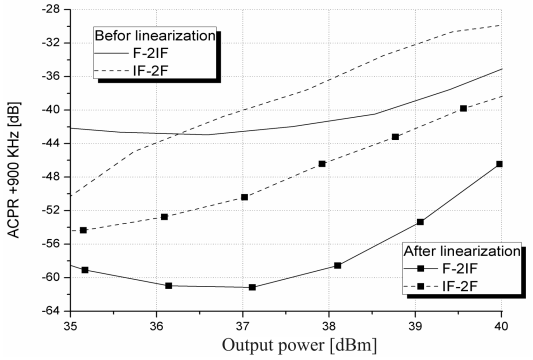

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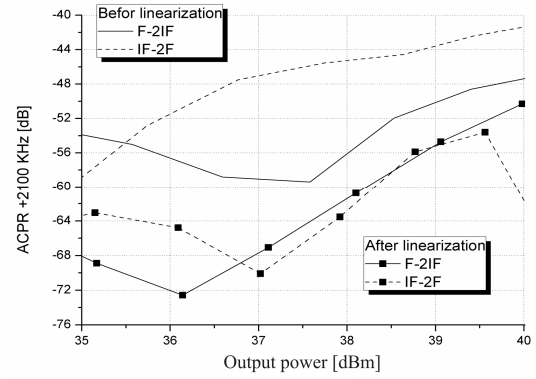
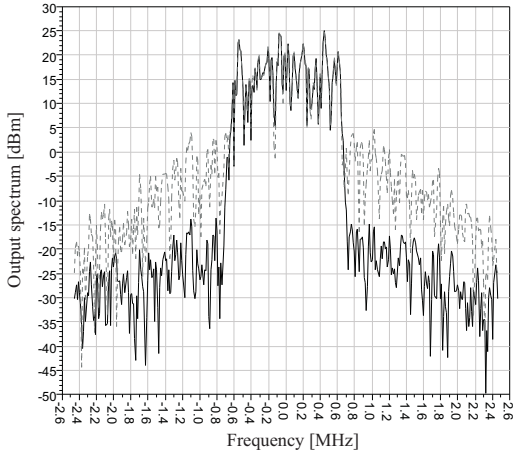


d)

Fig. 4 ACPR of HCC three-stage Doherty amplifier in a power range, before and after linearization, at offsets from carrier frequency: a) -900kHz; b)-2100kHz; c) +900kHz; and d) +2100kHz, in case of transistor periphery 1:2.5:2.5

These results are compared to the case when linearization is not carried out. The presented results relate to the case when the amplitudes and phases of IM2 and IM4 signals are adjusted on the optimal values for 23dBm and 26dBm input power in the same and different transistor periphery, respectively. It is evident from Fig. 3 and 4 that the linearization with the proposed approach gives satisfactory results in ACPR improvement at ±900kHz offset. After linearization, class-F-2IF amplifier has obviously lower ACPR at ±900kHz offset than class-IF-2F in the whole power range. When ACPR at ±2100kHz is considered, it is evident that there is an improvement but it is hard to say which configuration is better.

The ACPRs obtained in simulation before and after the linearization for CDMA digitally modulated signal are compared in Table II. Additionally, the output spectra attained in simulation before and after the linearization for HCC class-IF-2F, with carrier output power 35dBm (same transistor periphery) and 38dBm (different peripheries) are shown in Fig. 5.



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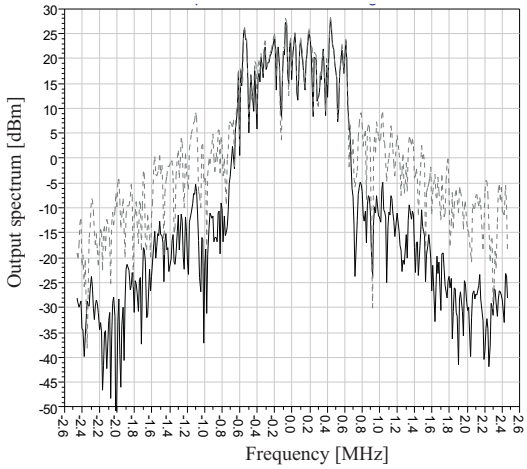
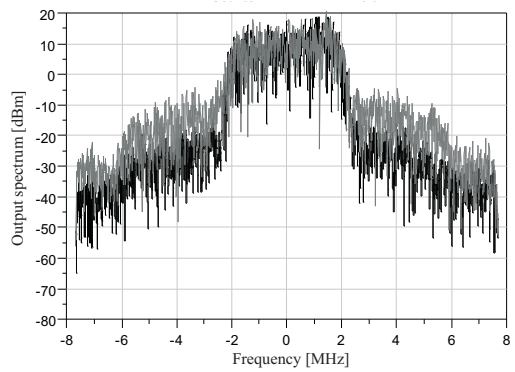


b)

Fig.5 Simulated output spectrum for HCC class-IF-2F three-stage Doherty amplifier for CDMA digitally modulated signal before (dashed line) and after the linearization (solid line) for: a) same; b) different transistor periphery

Table II. Average output power and ACPR at offsets ±900kHz and ±2100kHz from carrier frequency for three-stage Doherty amplifier before and after the linearization for HCC class-IF-2F in case of CDMA signals and HCC class-F-2IF in case of CDMA and WCDMA signals

Type	ACPR (dB)			ACPR (dB)			Fun. signals (dBm)	
HCC	Offset (MHz)	Bef.	Aft.	Offset (MHz)	Bef.	Aft.	Bef.	Aft.
LDMOSFET size ratio 1:1:1, Input power 23dBm								
Class-IF-2F	+0.9	-36.31	-56.43	+2.1	-45.95	-59.54	35.18	35.12
	-0.9	-34.52	-52.88	-2.1	-44.37	-65.82		
Class-F-2IF	+0.9	-36.40	-53.34	+2.1	-46.29	-61.48	35.00	34.93
	-0.9	-35.00	-56.68	-2.1	-44.82	-65.78		
	without tantalum capacitors			with tantalum capacitors				
	+5	-26.69	-37.35	+5	-30.38	-45.27	36.53	35.77
	-5	-25.99	-36.97	-5	-28.94	-47.06	36.54	35.97
LDMOSFET size ratio 1:2.5:2.5, Input power 26dBm								
Class-IF-2F	+0.9	-34.57	-49.98	+2.1	-50.42	-69.12	38.63	37.92
	-0.9	-33.49	-46.43	-2.1	-44.58	-63.53		
Class-F-2IF	+0.9	-39.25	-54.64	+2.1	-51.98	-66.39	38.53	38.1
	-0.9	-40.48	-58.57	-2.1	-51.96	-60.75		



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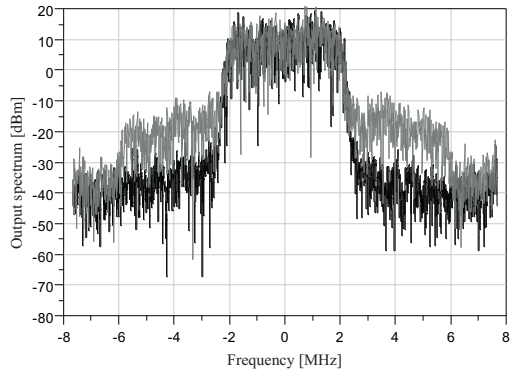


b)

Fig. 6 Simulated output spectrum for HCC class-F-2IF three-stage Doherty amplifier for WCDMA digitally modulated signal before (dashed line) and after the linearization (solid line) for the same transistor periphery a) without tantalum capacitors; b) with tantalum capacitors.

Linearization results for wideband digitally modulated signal WCDMA with average carrier output power of 36dBm (5dB backoff) in case of three-stage class-HCC-F-2IF Doherty amplifier are shown in Fig. 6 for the cases with and without additional tantalum capacitors. The capacitors are included at the input and output of transistors in amplifying cells [14] in order to short low frequency signals, of MHz order, descending memory effect. ACPR at ±5MHz offsets from the carrier frequency is given in Table II. One can notice that better linearity was accomplished when tantalum capacitors are in Doherty amplifier. ACPR is lower in reference to Doherty configuration without capacitors, approximately 3dB before and 8dB after the linearization.

V. THEORETICAL ANALYSIS OF LINEARIZATION TECHNIQUE APPLIED IN EXPERIMENT

Theoretical analysis of the proposed linearization approach is based on the nonlinearity of drain-source current of LDMOS in amplifier circuit which is expressed by a polynomial model [19], [20] under the assumption of neglecting the memory effect, as represented by (1).

$$\begin{aligned} i_{ds}(v_{gs}, v_{ds}) &= K_{10}v_{gs}(t) + K_{20}v_{gs}^2(t) + K_{30}v_{gs}^3(t) + \\ &+ K_{40}v_{gs}^4(t) + K_{50}v_{gs}^5(t) + K_{11}v_{gs}(t)v_{ds}(t) + \\ &+ K_{21}v_{gs}^2(t)v_{ds}(t) + K_{12}v_{gs}(t)v_{ds}^2(t) + \ldots \end{aligned} \quad (1)$$

Equation (1) connects the nonlinearity of the drain-source current i_{ds}, in reference to voltage v_{gs} between gate and source, which is represented by the coefficients K_{10} to K_{50}. Higher order nonlinear terms K_{40} and K_{50} are included into the equation according to the analysis performed in [20] that favours the terms of output current as function of v_{gs} up to the fifth-order. The nonlinearity of drain-source current in terms of voltage between drain and source, v_{ds}, which is expressed by the coefficients K_{01} to K_{03}, is assumed to have a negligible contribution to the intermodulation products according to [19]

and [20], so that they are omitted from the equation. However, the equation encompasses "mixing" terms K_{11}, K_{12} and K_{21}.

The drain-source current at IM3 and IM5 frequencies can be written by (2) and (3), where ρ_2, φ_2, ρ_4 and φ_4 stand for amplitudes and phases of the IM2 and IM4 signals put at the amplifier input, whereas $\rho_2^{(F)}$, $\varphi_2^{(F)}$, $\rho_4^{(F)}$ and $\varphi_4^{(F)}$ are amplitudes and phases of IM2 and IM4 signals that exist at the amplifier output due to both an inherent nonlinearity of transistor and transferred signals from the input.

The signal distorted by the cubic term of the amplifier, K_{30}, is included into analysis by (2) as the first term. The cubic term is considered as a dominant one according to [19] and [20] in causing IM3 products and spectral regrowth. The term K_{20} (second term) is created by the gate-source voltage of fundamental signal and voltage of second harmonic fed at the amplifier input. The mixing product of the fundamental signal and second harmonic appearing at the amplifier output is expressed as the third term. Additionally, the fundamental signal at the output of amplifier mingles with the second harmonic injected at the amplifier input generating fourth term. The amplitude of output voltage at fundamental signal frequency that is 180° out of phase in reference to the input signal is denoted as ρ_1. Third and fourth terms can be neglected for lower signal power. In case of higher power, they may reduce each other. The mixing terms between drain and gate, K_{12} and K_{21}, produce drain-source current at IM3 frequencies with the opposite phases, so that they reduce each other [19].

$$I_{ds}(j\omega)|_{IM3} \approx \left\{\left[\frac{3}{4}K_{30} + \frac{1}{4}K_{20}\rho_2 e^{-j\varphi_2} + \right.\right.$$
$$\left.+\frac{1}{4}K_{11}\rho_2^{(F)} e^{-j\varphi_2^{(F)}} - \frac{1}{4}K_{11}\rho_1\rho_2 e^{-j\varphi_2}\right]$$
$$\left.(V_B(j\omega)\otimes V_B(j\omega)\otimes V_B(j\omega))\right\}\otimes\frac{1}{2}\delta(\omega\pm\omega_0) \quad (2)$$

According to the previous analysis, it is possible to reduce spectral regrowth caused by the third-order distortion of fundamental signal by choosing appropriate amplitude and phase of the second harmonics (ρ_2 and φ_2).

The first term in (3) expressing the drain-source current of the fifth-order intermodulation products (IM5) is formed from the fundamental signals due to an amplifier nonlinearity of the fifth-order, K_{50}. The second term is the mixing product between the fundamental signal at amplifier input and IM4 signal inserted to its input, too. Therefore, the original IM5 product (the first term) can be reduced by adjusting the amplitude and phase of IM4 signals that are injected at amplifier input. The IM5 products are also expressed in terms of K_{30} coefficient-the third term in (3) made by reaction between two IM2 signals and fundamental one at the amplifier input. Also, the fundamental signal at the amplifier output reacts with the IM4 signal at the amplifier input over K_{11} term producing IM5 product (fourth term). The fifth term is made between the fundamental and IM4 signals at the amplifier output. All mixing terms which stand by K_{12} and K_{21} in (3) are generated due to reaction between two second harmonics and fundamental signal. The signals taken in consideration are observed at the input and output of amplifier. The K_{12} and K_{21} terms produce current at the frequencies of IM5 products with the opposite phases, so that they reduce each other. Consequently, their influence to the power of IM3 and IM5 products can be cancelled.

$$I_{ds}(j\omega)|_{IM5} \approx$$
$$\left\{\left[\frac{5}{8}K_{50} + \frac{1}{4}K_{20}\rho_4 e^{-j\varphi_4} + \frac{1}{8}K_{30}\rho_2^2 e^{-j2\varphi_2}\right.\right.$$
$$-\frac{1}{4}\rho_1 K_{11}\rho_4 e^{-j\varphi_4} + \frac{1}{4}K_{11}\rho_4^{(F)} e^{-j\varphi_4^{(F)}}$$
$$+\frac{1}{8}K_{12}\rho_2^{(F)2} e^{-j2\varphi_2^{(F)}} - \frac{1}{8}K_{12}\rho_1\rho_2\rho_2^{(F)} e^{-j\left(\varphi_2+\varphi_2^{(F)}\right)}$$
$$\left.+\frac{1}{8}K_{21}\rho_2\rho_2^{(F)} e^{-j\left(\varphi_2+\varphi_2^{(F)}\right)} - \frac{1}{8}K_{21}\rho_1\rho_2^2 e^{-j2\varphi_2}\right]$$
$$V_B(j\omega)\otimes V_B(j\omega)\otimes V_B(j\omega)\otimes V_B(j\omega)\otimes V_B(j\omega)\}$$
$$\otimes\frac{1}{2}\delta(\omega\pm\omega_0) \quad (3)$$

As in the case of IM3 products, third to fifth terms have negligible impact for lower power of the fundamental signals, while in case of higher power, it can be assumed that fourth and fifth terms cancelled each other. However, for higher power of the fundamental signal the second harmonics at the amplifier input are supposed to have greater amplitudes as well, so that mixing K_{30} term (the third term in (3)) influences the power of IM5 spectrum. Depending on the second harmonic phase at the amplifier input this term can increase or decrease IM5 products if IM4 signals injected at the amplifier input do not have enough power against the K_{30} term to control it.

VI. Experimental Results

We have been designed two-way Doherty amplifier in standard configuration [1]-[3], [5], [9] and realized it on FR4 substrate with Freescale's MRF281SR1 LDMOSFET (4-W peak envelope power) in carrier and peaking cells, as shown in Fig. 7. The second harmonics and fourth-order nonlinear signals at frequencies close to the second harmonics, which are generated at the output of the peaking amplifier, are extracted through the diplexer circuit [5] that was designed to separate the fundamental signals and signals for linearization.

The additional linearization circuit is presented in Fig. 8. It comprises from M/A-COM PIN diode variable attenuator MA4VAT2007-1061T, two Mini-Circuits 180° voltage variable phase shifters JSPHS-23+ to provide phase shift of 360° and high linear 2W power amplifier produced by Skyworks and denoted as SKY65120. The linearization circuit adjusts IM2 and IM4 signals in amplitude and phase before

they are inserted at the carrier amplifier input over the frequency diplexer. Linearization branch can vary power of the signals for linearization from -10dB to 7dB in reference to the generation point at peaking amplifier output.

S-parameters of Doherty amplifier obtained in simulation by ADS as well as the measured parameters are shown in Fig. 9. The figure compares the characteristics achieved in case of ideal lossless amplifier circuit (dashed line) and in case when losses and discuntinuity effects of tee-sections and banded microstrip lines are included into analysis [21]. One can notice that amplifier operational frequency is shifted from the design frequency of 1GHz to 1.006GHz in the fabricated amplifier.

The measured output spectra of Doherty amplifier before and after applying the linearization for two sinusoidal signals at 8dBm input power at frequencies 1.0065GHz and 1.0075GHz are compared in Fig. 10. Two input signals are generated by local oscillators that limit upper signal power slightly above 14dBm, which is 7dB below maximal power level for the transistors utilized.

The fundamental signal output power is about 19.96dBm before and 19.35dBm after the linearization. The third-order intermodulation products at frequencies 1.0055MHz and 1.0085GHz are lessened by linearization from -8dBm to -16dBm and -13dBm, respectively. As far as the fifth-order intermodulation products are concerned, the reduction is around 6dB at frequencies 1.0045MHz and 1.0095GHz. In simulation, two-way Doherty amplifier is tested for two sinusoidal signals at frequencies 990.5MHz and 991.5MHz, where designed amplifier circuit has maximal gain. As the result, IM3 products are lower by 9dB and 6dB, whereas IM5 products become worse by 2dB in case of 20dBm fundamental signal output power.

The results from Fig. 11 show the effects of two-way Doherty amplifier linearization accomplished for the output power ranging from 10dBm to 26dBm. These results are compared to the case when linearization is not carried out. Fig. 11a) relates to the power reduction of IM3 at 1.0055GHz (IM3-) and 1.0085GHz (IM3+), whereas Fig. 11b) shows results connected to the IM5 products at 1.0045GHz (IM5-) and 1.0095GHz (IM5+).

It is evident from these figures that the linearization with the proposed approach gives satisfactory results in improvement of IM3 products for the power range up to approximately 18dBm and becomes asymmetrical at higher power. However, IM5 products decrease slightly at lower power levels whereas they get worse at higher power range considered, though IM5 products are kept at lower power level in reference to the linearized IM3 products. According to (2) and (3), IM2 and IM4 signals can reduce both IM3 and IM5 products that depends on the relations between amplitudes as well as phases of the IM2 and IM4 signals generated at the peaking amplifier output. However, when required relations are not fulfilled, only one kind of intermodulation products can be reduced sufficiently.

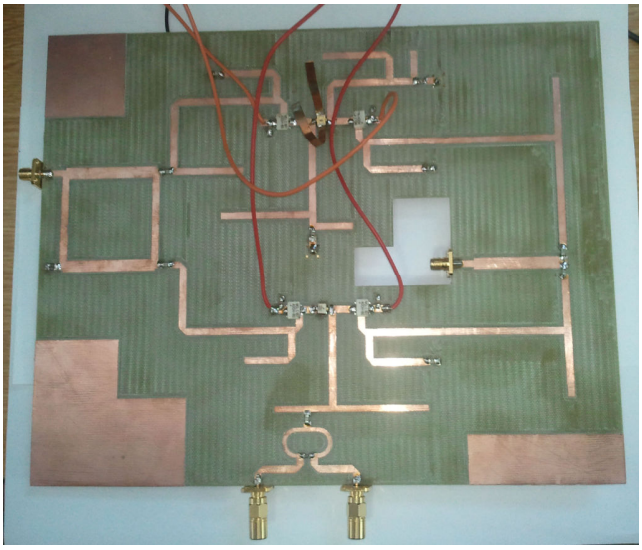


Fig. 7. Realized two-way Doherty amplifier

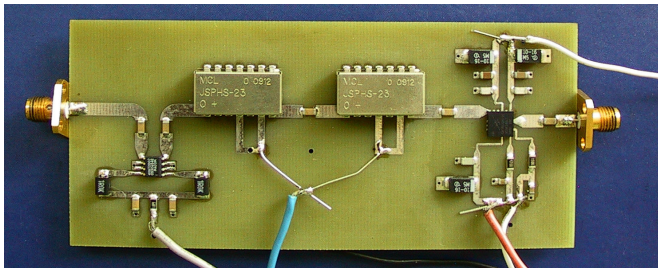


Fig. 8. Realized linearization circuit

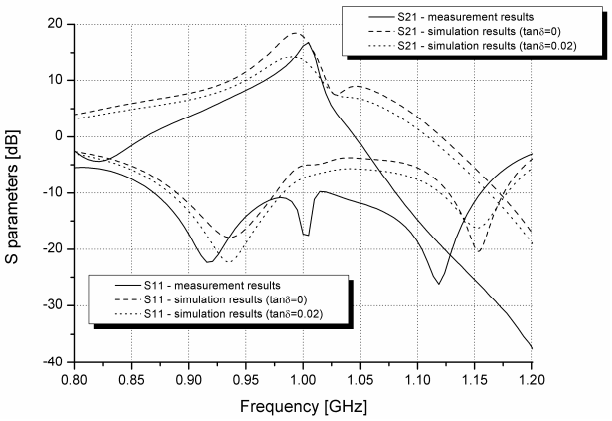


Fig. 9. S-parameters of two-way Doherty amplifier

Doherty amplifier drain efficiency (DE) obtained in simulation for ideal circuit case without losses, the simulated characteristic gained for the loss microstrip circuit with included discontinuities and the measured values are compared in Fig. 12. The good agreement can be observed between curves relating to the real simulated Doherty amplifier and experimental results up to 34dBm power that is maximal level that can be reached by the available laboratory equipment which generates input signals for experiment. At this power level, there is a maximal discrepancy between the simulated and measured result of 5%. The maximal efficiency achieved

by the realized circuit is 32.7%.

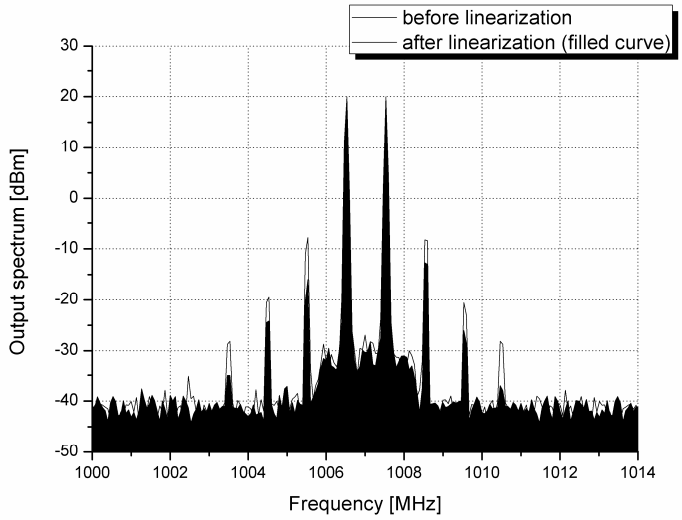
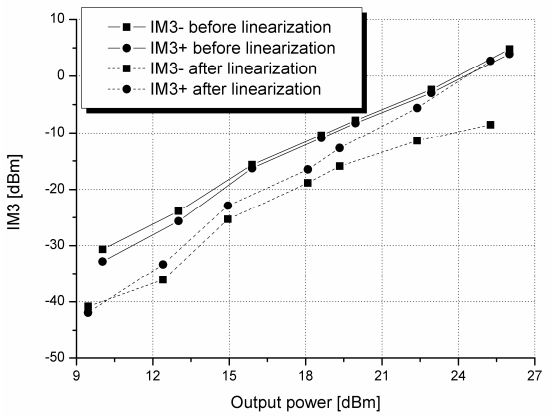
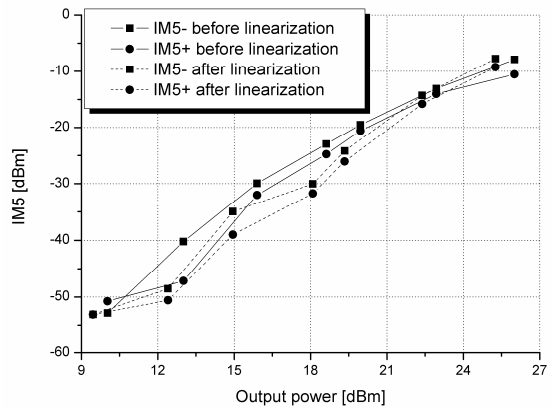


Fig. 10. Measured output spectra for 8dBm input power of fundamental signals; before and after linearization (filled curve)



a)



b)

Fig. 11. Measured intermodulation products before and after linearization of two-way Doherty amplifier for a power range: a) third-order; b) fifth-order products

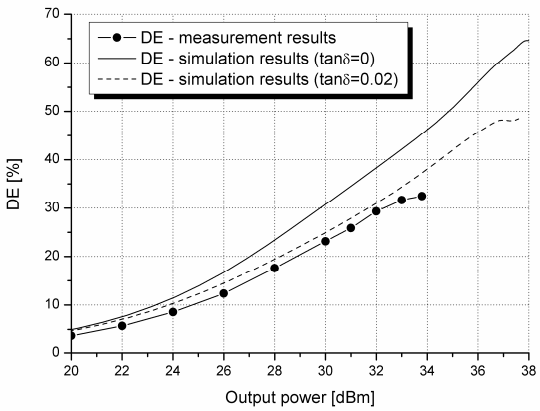


Fig. 12. Drain efficiency of two-way Doherty amplifier

VII. CONCLUSION

This paper presents the linearization effects of technique that uses second harmonics and fourth-order nonlinear signals at frequencies that are close to the second harmonics on the simulated three-stage and realized standard two-way Doherty amplifiers. The amplifiers have been designed with LDMOSFETs in carrier and peaking cells with the same transistor periphery and moreover, in case of three-stage amplifier, transistor size ratio 1:2.5:2.5 has been analyzed. Amplifying cells are loaded with the frequency diplexer at the outputs that, in case of three-stage amplifier, additionally includes harmonic control circuit. It enables the optimal impedance for adequate power of the signals for linearization as well as a short circuit for the third harmonics at the output of the carrier cell and an open circuit at the output of the peaking cells. For this configuration of three-stage Doherty amplifier (denoted as HCC class-IF-2F) the linearization has been carried out with the simultaneous injection of the second harmonics and fourth-order nonlinear signals at the input and output of the carrier cell. The linearization approach achieves very good results in the reduction of both third- and fifth-order intermodulation products retaining the high efficiency of Doherty configuration. Obtained results have been compared to three-stage Doherty amplifier in class-F-2IF (the optimal impedance for signals for linearization and the open circuit for third harmonics at the output of carrier cell, whereas they are shorted at the output of the peaking cells). Moreover, the linearization technique is applicable for wideband WCDMA signal if tantalum capacitors are added at transistor input and output of Doherty cells, which has been considered for class-F-2IF with the same transistors.

This paper also presents for the first time the experimental verification of two-way Doherty amplifier linearization by simultaneous injection of the second harmonics and fourth-order nonlinear signals at the input of carrier amplifier. The linearization approach achieves very good results in reduction of third-order intermodulation products, even for wider power range. When the fifth-order intermodulation products are concerned, the mild suppression is observed at lower power level, however these products become worse at higher power range. Measurements are constrained by laboratory equipment

to lower power that is 7dB below the maximal available power of transistors utilized.

We would point out that the crucial matter in the linearization approach used for Doherty amplifier linearization is the possibility to exploit the peaking amplifier as source of signals for linearization and therefore avoid the necessity for additional nonlinear sources that will increase the circuit complexity and total energy consumption.

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