Computationally Efficient Analytical Crosstalk Noise Model in RC Interconnects

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***Abstract*—**This paper presents an accurate, fast and simple closed form solution to estimate crosstalk noise between two adjacent wires, using RC interconnect model in two situations: simple resistance as driver and short channel CMOS inverter as a driver. The salient features of our proposed models include minimization of computational overhead, elimination of adjustment step to predict the peak amplitude and pulse width of the noise waveform. Numerical calculations are compared with SPICE simulation and other metrics by plotting the noise voltage verses time. Based on our proposed models, we derive analytical delay models due to RC interconnect in each case. Finally we formulate energy dissipation of the RC coupled interconnects in both the cases using our proposed metrics. Experimental results indicate that our models are closely comparable with SPICE simulation, with an average estimation error of 3.366%.

***Keywords*—** Analytical Delay model, Crosstalk Noise, Energy Dissipation Estimation, Non-linear Driver, RC interconnects.

I. Introduction

In addition to the reduction in chip area, the scaling down of the feature size in deep submicron technology results in performance degradation of VLSI circuits such as logic failure, timing delay, unwanted coupling voltage between two adjacent wires. In the current technology, Crosstalk noise has become significant in the performance of VLSI circuits. Crosstalk noise exhibits a negative impact on the reliability of the VLSI circuits. Now it is time to VLSI designers to examine the crosstalk noise effects in their designs, so that they are free from noise. Cross talk noise modeling approaches are loosely classified into two categories based on their tradeoff between accuracy and efficiency [1]. They are analytical modeling and SPICE simulation. Analytical modeling is preferred because simulation using SPICE is always computationally expensive and time consuming, with the modern designs containing millions of transistors and wires. In addition, this estimation must be done at the early stage of the designs. Because detecting coupling induced problems at the late stage of the designs may implicate difficulties as most of the layout is completed and it may not be possible to modify floor planning, placement and routing at that stage [2]. Analytical modeling is developed based on two techniques, Elmore delay model and moment matching technique. Moment matching technique is quick to provide peak amplitude of noise voltage. However it has two drawbacks: Deriving solution is difficult, as it needs Laplace and inverse Laplace transform. Using Moment Matching method, it may take more than one day to complete the noise in a modern Micro Processor [3]. The summations of time constants is determined at each capacitor in the second technique, Elmore delay model. Devgan[4] & Heydari[5] proposed analytical models based on Elmore delay model. Analytical model of [4] is a simple mathematical expression to estimate the peak amplitude of the cross talk noise. However this model has several disadvantages: It is less accurate; it does not consider the parasitic parameters of aggressor net to compute crosstalk noise; it cannot provide complete time domain waveform. The model in [5] is a very effective mathematical model to estimate crosstalk noise voltage waveform in time domain. This metric considered the disadvantages of Devgan's model. They computed time constant of RC interconnect model at each node by considering parasitic parameters of both aggressor and victim nets. Still this metric also has several drawbacks: They have adjusted the time constant of RC interconnect by multiplying ξ (1.01 to 1.09) with the time constant. Secondly, to compute noise voltage waveform in time domain, they considered Devgan's result as the steady state value, which itself is highly inaccurate at an average error of 644% ; Finally to compute crosstalk noise, it takes two iterations, i.e., One iteration to find time constant (τ_d) and another one to get steady state value by using Devgan's metric. [6] proposed an accurate solution to crosstalk noise voltage waveform in time domain. This model addressed all the drawbacks of [5], namely adjustment of the time constant of RC interconnect by multiplying ξ with the time constant; Passing two iterations to compute noise voltage and considering a highly inaccurate voltage as the steady state value. With reference to non-linear driver, the recent works are as follows: Huang [7] proposed a complete set of analytical models for signal delay, rise time and voltage overshoot for a non-linear driver based RC interconnect. But all their mathematical expressions are complex. Still their closed form expression for output voltage has considered only one region of operation for CMOS inverter. The main limitation of Huang's metric is not considering: Coupling effects of adjacent wires and complete non-linear nature of CMOS inverter while deriving expressions for rise time and voltage waveform at the gate output. [8] presented a dual ramp driver model for RLC interconnect using piecewise approximation to the characteristics of CMOS inverter, which does not consider cover the complete range of operation of CMOS inverter. From above discussion, it is clear that the models of [7] & [8] do not provide complete non-linear nature of CMOS inverter. These models are likely to give large errors, while estimating crosstalk noise in a short channel CMOS inverter based RC interconnect. This paper presents two noise metrics: one is referred to linear driver as source and another one is based on non-linear driver, based on [6], which does not account for non-linear nature of the driver resistance. Our proposed models are closed form solutions to predict peak amplitude and pulse width of crosstalk noise voltage of an RC interconnect, which address all the drawbacks of previous metrics [4], [5], [7] & [8]. Our proposed noise metric, in the first case has a closed form expression, depends on circuit parameters of both aggressor and victim nets and rise (fall) time of the input signal. Our model presents a noise waveform in time domain which is further compared with SPICE simulation results. In the second

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case, we propose a realistic mode, which accounts for non-linear driver and the time constant as in [6]. As our proposed mathematical expressions, to compute voltage at any node of aggressor victim net, need peak amplitude of its corresponding predecessor node of aggressor wire, it computes the voltage at that node with the same expression in the previous cycle and our results are closely matched with SPICE simulation results. This proposed second noise metric has a closed form expression, depends on circuit parameters of aggressor and victim nets, strength of the driver, rise time of aggressor and coupling capacitance between the two adjacent wires. As in the current technology, the interconnect effects like delay and energy dissipation due to crosstalk are significant, we subsequently investigate these effects elaborately. After obtaining analytical models for complete time domain noise voltage using those models, we develop analytical delay and energy dissipation estimation models due to RC interconnects.

Sections 2 reviews fundamentals of interconnects, Next Devgan's metric & Heydari's metric are discussed. Then we introduce our metric, referred to linear resistance as driver, then our non-linear driver based proposed metric is presented. Comparison between our models and SPICE simulations are explained. Our proposed analytical delay and energy dissipation estimation models are followed on each metric. Finally we present concluding remarks.

II. Review Of Interconnects

In deep submicron technology, VLSI circuits usually consist of several parallel bus structures (collection of adjacent wires) result in significant parasitic coupling effects. These coupling effects produce interference, between signals is referred to as Crosstalk noise [9]. These effects may be capacitive or inductive. In this paper, we restrict our attention to only capacitive effects. Crosstalk effects can lead to logic failure, increased power dissipation and timing degradation in Digital system. Consider a two minimally separated adjacent wires as shown in Fig.1. A step input, with t_r, rise time is applied to aggressor net, which is propagated to the far end and is in the exponential shape due to the presence of R_a and C_a. Though '0 V' (GND) is applied to victim net, because of coupling capacitance 'C_c', a cross talk noise voltage 'V_V' will be appeared at the far end of victim net, for a duration of 't_p'. The parasitic RC interconnect model of Fig.1 is given in Fig. 2.

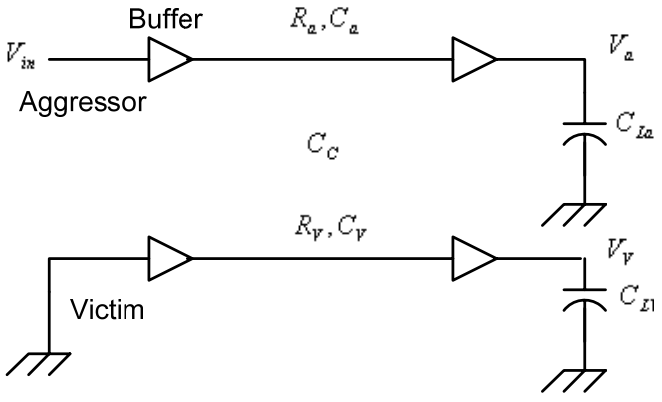


Fig.1.Two parallel minimally separated wires.

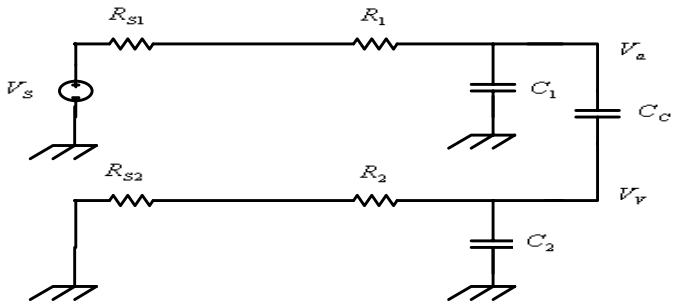


Fig.2. Lumped RC interconnect model of two parallel wires.

The driver of aggressor node is modeled as a voltage source V, series resistance R_{S1}. R_{S2} is the effective victim node driver resistance to the ground node. C_a & C_b are effective capacitances of the wires to ground node. C_c is effective coupling capacitance between two adjacent wires. Theoretically, V_V must be zero. However, due to parasitic coupling effects V_V will be present.

Mathematically

$$V_V = V_{DD}(1-e^{-t/\tau})u(t) \quad (1)$$

'τ' is the time constant.

We first review Devgan's & Heydari's metrics and their drawbacks in estimating cross talk noise in RC circuits. Then we derive a new analytical expression to capacitive coupling model, which eliminates the drawbacks of Devgan's & Heydari's metrics.

A. Devgan's Metric

To better understand this approach, consider a pair of capacitively coupled second order RC circuit, as shown in Fig.3. R_{S1} & R_{S2} represent the resistances of the input source, which are on resistances of line drivers.

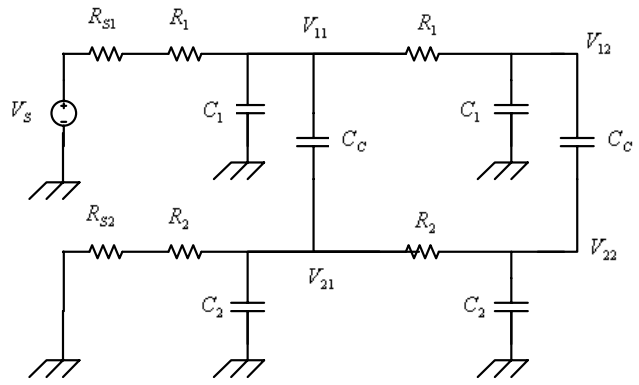


Fig.3.A pair of two capacitively coupled II order RC Circuit

Consider typical values of these parameters i.e., assume that

C_1 = 60 fF, C_2 =120 fF, R_2 =100 Ω, R_1 =20 Ω, C_c = 180 fF, R_{S1} =100 Ω, R_{S2} = 150 Ω, t_r =0.1 nsec.

From the SPICE simulation, the reported value of voltage V_{22} is 0.3649 V.

Devgan's metric for the same as follows

$$V_{21,SS} = \left(2(R_2 + R_{S2})\right)C_C\,(V_{DD} / t_r) \tag{2}$$

$$V_{22,SS} = (3R_2 + 2R_{S2})C_C\,(V_{DD} / t_r) \tag{3}$$

Using (3) $V_{22,SS}$ is 1.404V. The estimated error is 284.76 %. When the input signal rise time is small, the crosstalk waveform rolls down quickly and consequently error becomes unacceptably large.

B. Heydari's Metric

The distributed RC model proposed by Heydari is shown in below Fig 4.

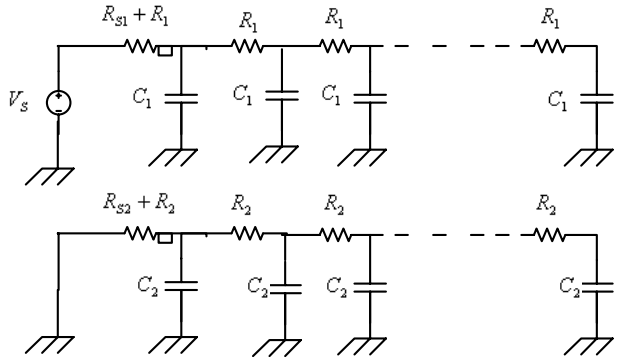


Fig.4.Heydari's Model of Distributed RC Interconnect.

To compute the noise peak value, the capacitive crosstalk noise at every node of victim net is a rising exponential function during time interval of input.

$$V_{2,MAX} = V_{2,SS}\,(1 - e^{-t_r / \tau_{dj}}) \tag{4}$$

for j = 1,2,……N

τ_{dj} is the time constant of the '*j*'th node voltage in the victim net and V_{2SS}, steady state crosstalk noise voltage measured using Devgan's metric. The time constant at each node is equal to the summation of individual time constants due to each of the capacitances.

Considering 'ξ' as constant factor for the delay increase due to non-zero i.e., finite input value, which ranges in [1.00, 1.02], Payam has considered 'ξ' to be 1.09. Now time constant at node '*j*'

$$\tau_{dj} = \xi[R_{1jeq}C_{cj} + \sum_{k=1}^{j}(R_{1keq}(C_{ck} + C_{1k}) + R_{2keq}(C_{2k} + C_{ck}))] \tag{5}$$

For j = 1, 2 ….N,

where $R_{1jeq} = R_1(j) + R_{S1}$ & $R_{2jeq} = R_2(j) + R_{S2}$

As special case, consider two second order capacitively coupled RC network, as in Fig. 4 and the same physical parameters.

Applying (4) & (5), the closed form expressions for peak value of the victim net are

$$V_{21} = V_{21,SS}\,(1 - e^{-t_r / \tau_{d1}}) \tag{6}$$

Where

$$\tau_{d1} = \xi[(R_1 + R_{S1})(C_C + C_1) + (R_2 + R_{S2})(C_C + C_2)]$$

$$V_{22} = V_{22,SS}\,(1 - e^{-t_r / \tau_{d2}}) \tag{7}$$

Where

$$\tau_{d2} = \xi[(3R_1 + 2R_{S1})(C_C + C_1) + (3R_2 + 2R_{S2})(C_C + C_2) + (2R_1 + R_{S1})C_C]$$

Applying the same physical parameters, considered for Devgan's metric, V_{22} is computed to be 0.404 V. The estimated error is 10.71% compared SPICE simulation.

C. New Metric for Crosstalk Estimation

Careful investigation of these metrics and SPICE simulation shows that the computation of time constant is inaccurate. Mainly Heydari has done one adjustment by multiplying 1.09 (ξ) to the calculated time constant. Another error in his metric is calculation of peak value of victim node is based on the steady state value, calculated using Devgan's metric, which itself is 644% error, compared SPICE simulation. Further, to compute peak value of victim node, we must first find out steady state value using Devgan's metric in first iteration, followed by computing peak value using (4), in the second iteration, which results in slow in computation. These three issues are mainly responsible for inaccuracy of Heydari's metric to estimate cross talk noise.

In this paper, we propose a closed form solution to address all these issues and still more accurate solution than Heydari's and Devgan's metrics. Our contribution is mainly based on the following concept. The time constant due to each capacitance is obtained by calculating equivalent resistance seen across each capacitance, with all other capacitances open circuited. Consider the following equivalent circuit in Fig. 5. The time constant at '*j*'th node of aggressor net sees two capacitances C_i & C_c, where as '*j*'th node of victim net sees two capacitances C_c & C_2 and replace all other capacitances with open circuited. The circuit model is presented in Fig. 5.

Hence the time constant of the '*j*'th node of aggressor net, τ_{aj} is given by

$$\tau_{aj} = R_{1j}C_{1j} + C_{Cj}(R_1 + R_{2jeq}) \tag{8}$$

Where R_{1j} is resistance of '*j*'th node of aggressor net.

And the time constant of '*j*'th node of victim net, τ_{Vj} is given by

$$\tau_{Vj} = R_{2jeq}(C_{Cj} + C_{2j}) \tag{9}$$

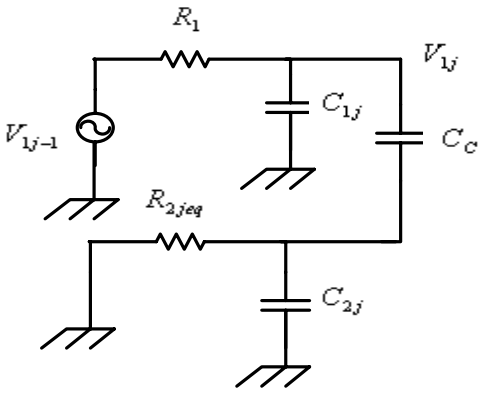


Fig.5. Equivalent Circuit Model to Compute Time- Constant of the '*j*'th node of Aggressor and Victim nodes**.**

Where $R_{2\,jeq}$ is resistance of '*j*'th node of victim net, which is equal to ($R_2 . j + R_{S2}$).

By considering (8) & (9) and Fig 5, the voltages at the node of aggressor and victim nets are as follows

$$V_{1j\max} = V_{1j-1\max}(1-e^{-t_r/\tau_{aj}}) \tag{10}$$

Where $V_{1j-1\max}$ is peak value of (*j*-1) node of aggressor net which is computed with same expression recursively considering τ_{aj-1} as in (8).

$$V_{2j\max} = V_{1j\max}(1-e^{-t_r/\tau_{Vj}}) \tag{11}$$

The above expressions are much effective, simple and accurate to estimate peak values of voltages at aggressor and victim nets. To compute peak values of voltages at any node of aggressor & victim nets, these expressions need only the peak value at its predecessor node of aggressor net, unlike depends on steady state value using Devgan's metric. These expressions eliminate the adjustment step also. Further this analytical model does not need steady state value using Devgan's metric, to compute peak voltages at any node. Within one iteration, at all nodes of aggressor and victim nets can be computed using (10) & (11) recursively considering the respective time constants using (8) & (9). To verify the accuracy of our model to estimate voltages at aggressor and victim nets using (10) & (11), we consider second order RC network, with same parameters, as Devgan's and Heydari's metrics.

Our proposed second order RC model is presented in Fig. 6.

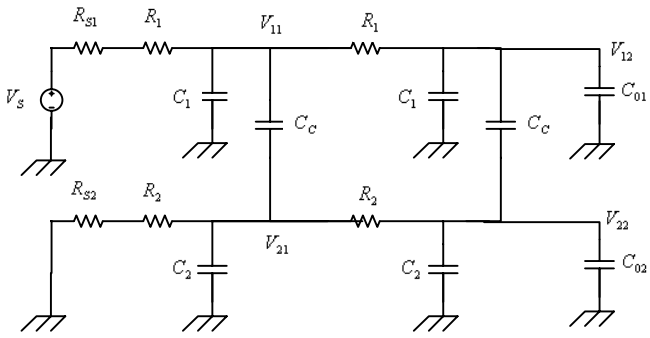


Fig.6. Proposed second order RC interconnect model

From (8) & (9), Time constant at first node of aggressor net is given by

$$\tau_{a1} = (R_1 + R_{S1})C_1 + (R_1 + R_{S1} + R_2 + R_{S2})C_C \tag{12}$$

Time constant at second node of aggressor net is given by

$$\tau_{a2} = R_1C_1 + (R_1 + 2R_2 + R_{S2})C_C + (2R_1 + R_{S1})C_{01} \tag{13}$$

Time constant at second node of victim net,

$$\tau_{V2} = (2R_2 + R_{S2})(C_C + C_2 + C_{02}) \tag{14}$$

Finally from (11) & (12), the voltages at 1st and 2nd nodes of aggressor are given by

$$V_{11} = V_{DD}(1-e^{-t_r/\tau_{a1}}) \tag{15}$$

$$V_{12} = V_{11}(1-e^{-t_r/\tau_{a2}}) \tag{16}$$

Further the voltage at 2nd node of victim net is given by

$$V_{22} = V_{12}(1-e^{-t_r/\tau_{V2}}) \tag{17}$$

The value of V_{22} computed to be = 0.379V.The estimation error of 3.86 % is reported, compared to SPICE simulation of V_{22} .

To prove the consistency of our metric, we conduct an experiment on a multistage RC network, to compare Devgan, Heydari and our proposed models with SPICE simulation. We performed a number of experiments on a two line structure in a 130nm CMOS technology. The coupled length of adjacent interconnects are varied from 200µm to 5mm. The supply voltage is 1.3V. Results are reported for a range of rise time between 30 ps to 200 ps and victim and aggressor driver resistances vary between 20 Ω to 2.5 K Ω. Table I contains these comparisons. The mean and maximum error values are reported in Table II. Table I and II clearly show that high accuracy of our model compared to other approaches. Further, our proposed model results in an average estimation error of 3.36 %, compared to SPICE simulation. Our metric is reported to be better than Heydari's metric, whose average estimation error is 51.28% and Devgan's metric, whose average estimation error is 644%. It is evident that static CMOS logic circuit can sustain the signals, without any loss, in the presence of Crosstalk Noise. However, it tends to cause an increase in propagation delay on victim net.

The complete Noise Waveform can be as follows

$$V_2(t) = V_1(1-e^{-t/\tau_{Vj}}) \qquad 0 < t \le t_r$$

$$= V_{2\max}e^{-(t-t_r)/\tau_{Vj}} \qquad t > t_r \tag{18}$$

This expression gives complete picture about noise behavior. This closed form expression enables the designers to try alternative solutions to minimize noise. Fig.8. Compares our metric (18) with SPICE simulation and Heydari's metric for capacitively coupled lines. Fig.7. shows the changes in crosstalk when the input rise time varies from 50 ps to 200 ps and all of geometric parameters are fixed. Fig.8 indicates that our plot is converging with the SPICE simulation at a particular instant of time. For long rise time Devgan's metric predicts accurately the peak amplitude of noise. Heydari's metric is best suited for lengthy interconnects. Finally, our metric is more accurate than the works done by Heydari & Devgan and is very close SPICE simulation.

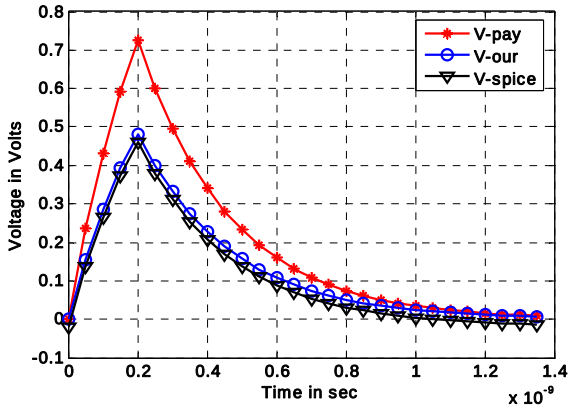


Fig.7.Crosstalk Noise waveform for two coupled transmission lines.

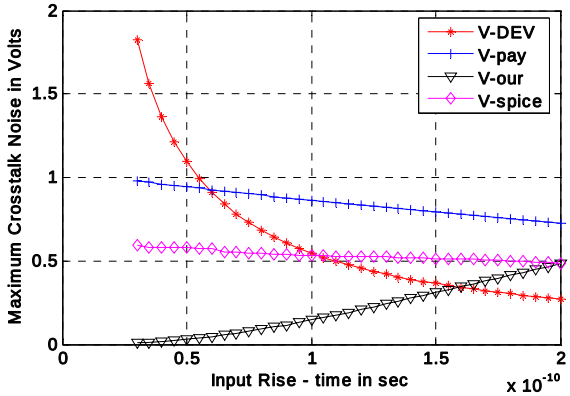


Fig.8. Maximum Crosstalk Noise versus input rise-time

Table I

Results of simulation on the two capacitively Coupled transmission lines using T-SPICE and our Proposed metric

R1 KΩ/ m	*Rs1 Ω*	*R2 KΩ/ m*	*Rs2 Ω*	*C1 pF/ m*	*C2 pF/ m*	*Cc pF/ m*	*Spice volts*	*Ours volts*
11.5	500	10.2	2500	60	64	100	0.094	0.096
9.3	75	10	150	92	80	170	0.356	0.325
17	325	17	335	140	100	200	0.245	0.241
12	190	8.5	100	85	75	140	0.183	0.159
9.55	527	9.6	400	72	72	150	0.191	0.186
8.2	270	7	240	83	90	160	0.188	0.183
10	625	10	750	120	120	132	0.197	0.2
15	800	15	550	108	108	200	0.163	0.166
13	270	20	250	130	100	220	0.201	0.204
9	26	15	550	97	30	120	0.433	0.425
7	37	16	500	100	14	100	0.379	0.399
11	160	11	140	90	90	120	0.17	0.164
17	20	17	150	140	100	200	0.414	0.407
8	1200	4	85	110	200	300	0.049	0.048
10	20	1.8	2000	70	20	95	0.484	0.487

Table II

Percentage Error Comparison of other metrics and Our Proposed Metric

	%Error Devgan	*%Error Heydari*	*%Error Ours*
	1283	427	2.12
	335	1.4	8.71
	536	2.04	1.6
	555	19.12	13.1
	623	22.51	2.6
	644	18.61	2.65
	625	48.73	1.5
	679	57.66	1.84
	593	8.9	1.49
	248	23.32	1.8
	259	79.15	5.27
	693	2.94	3.5
	267	5.07	1.69
	2142	2	2
	180	50.82	0.62
Average	**644**	**51.28**	**3.366**
Minimum	180	1.4	0.62
Maximum	2142	427	13.1

D. Our Proposed Metric for a Short Channel CMOS Inverter based RC Interconnect

In this section, we derive our model using short channel CMOS inverter as a driver. The RC interconnect model in this case is shown in Fig.9.

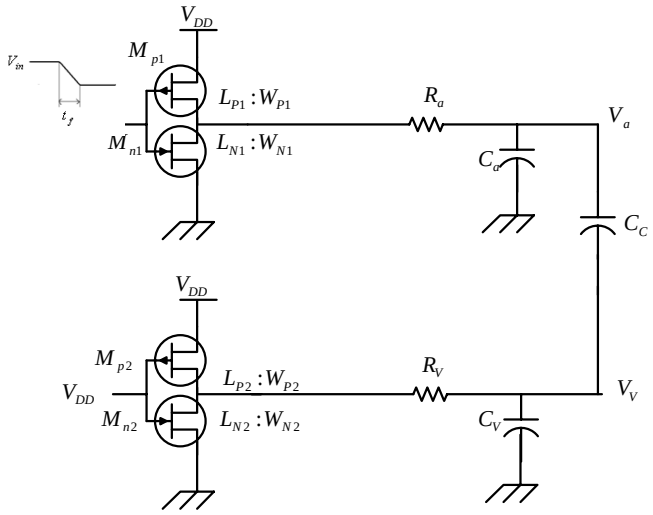


Fig.9. Transistor Based RC interconnect model

Consider Fig.9, aggressor inverter has $L_{P1}:W_{P1}$ and $L_{N1}:W_{N1}$ where as victim inverter has $L_{P2}:W_{P2}$ and $L_{N2}:W_{N2}$ V_{in} is applied input voltage with a t_f as fall time. R_a and R_V are wire resistances and C_a and C_V are corresponding ground capacitances of aggressor and victim nets respectively. C_C is coupling capacitance between aggressor and victim nets. Fig.10 illustrates the voltage waveforms at various nodes of aggressor & victim nets using SPICE simulation for Fig.9.

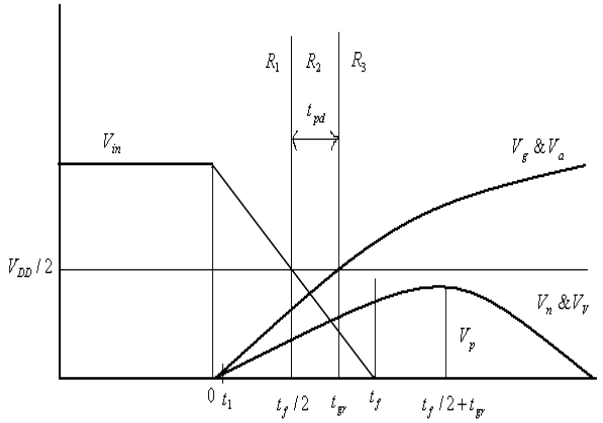


Fig.10. Voltage waveform at input and output of gate, far end aggressor and victim net

A step input with t_f fall time is applied at V_{in} node. In response, an exponential waveform is observed at V_g node with t_1 as its initial point. This waveform experiences a $V_{DD}/2$ point at t_{gr}, gate output rise time. The difference between t_{gr} and $t_f/2$ is defined as propagation delay of gate.

$$t_{pd} = t_{gr} - (t_f/2) \tag{19}$$

However, the noise waveform experiences its peak at $t_f/2 + t_{gr}$ and then decays to zero. In the absence of the inverter as driver, the noise waveform experiences its peak at rise time of input, whereas now its peak is further delayed by the propagation delay of the gate. Hence the noise waveform is same in shape in both cases, but is delayed by the propagation delay of gate, in its presence. According to voltage transfer characteristics of CMOS inverter, three different operating regions are distinguished in the time interval $[0, t_f/2 + t_{gr}]$. The regions of operations are summarized in Table III.

TABLE III
Summary of CMOS inverter behavior.

PMOS NMOS	SAT NONSAT	NONSAT SAT	NONSAT CUTOFF
V_{in}	$V_{DD} - \lvert V_{tp}\rvert$	$> V_{tn}$	$< V_{tn}$
V_{dsp}	$< V_{DD} + \lvert V_{tp}\rvert + V_{in}$	$> V_{DD} + \lvert V_{tp}\rvert + V_{in}$	Same
V_{dsn}	$< V_{in} - V_{tn}$	$> V_{in} - V_{tn}$	-
V_G	(21)	(23)	(23)
I_{dsp}	(20)	(22)	(22)
t	t_1 t_2	t_2 t_3	t_3 t_{gr}

The Table III illustrates the complete behavior of CMOS inverter at different instants of time. In practice however, CMOS inverter undergoes five different operation regions, R1, R2, R3, R4 and R5 [10]. To predict noise voltage, t_1 is considered as the starting point. As CMOS inverter spends a short duration in R3 region, the third and fourth intervals are merged together [11]. Hence the regions of operation are confined to three.

In Region '1'

$$I_{dsp} = \frac{W_p V_{sat} C_{ox} (V_{DD} - V_{in} - \lvert V_{tp}\rvert)^2}{(V_{DD} - V_{in} - \lvert V_{tp}\rvert) + E_{cp} L_p} \tag{20}$$

V_g can be computed using (21)

$$\frac{W_n}{L_n} \frac{\mu_n C_{ox}}{\left(1 + \frac{V_{out}}{E_{CN} L_N}\right)} \left[(V_{in} - V_{tn}) V_{out} - \frac{V_{out}^2}{2} \right] = \frac{W_p V_{sat} C_{ox} \left(V_{DD} - V_{in} - \lvert V_{tp}\rvert^2 \right)}{V_{DD} - V_{in} - \lvert V_{tp}\rvert + E_{cp} L_p} \tag{21}$$

For a given V_{in}, V_{out} can be computed, which is V_g.

In Region '2'

$$I_{dsp}=\frac{W_p}{L_p}\frac{\mu_p C_{ox}}{1+\frac{V_{DD}-V_{out}}{E_{cp}L_p}}\left[\left(\left(V_{DD}-V_{in}-\left|V_{tp}\right|\right)V_{DD}-V_{out}\right)-\frac{\left(V_{DD}-V_{out}\right)^2}{2}\right] \quad (22)$$

Now V_g can be computed, for a given V_{in}, V_{out} in (23), which is V_g.

$$\frac{W_N V_{sat} C_{ox}\left(V_{in}-V_{tn}\right)^2}{\left(V_{in}-V_{tn}\right)+E_{CN}L_n}=I_{dsp} \quad (23)$$

I_{dsp} Is considered from (22) [9]

$$t_1=\frac{V_{DD}-\left|V_{tp}\right|}{V_{DD}}t_f \quad (24)$$

$$t_2=\frac{\left(V_{out}+V_{tp}\right)}{V_{DD}}t_f \quad (25)$$

$$t_3=\frac{V_{tn}}{V_{DD}}t_f \quad (26)$$

μ_n - Mobility of electrons

μ_p - Mobility of holes

C_{ox} - Gate oxide capacitance per unit area

E_{CN} - Electric field for electrons

E_{CP} - Electric field for holes

V_{sat} - Velocity of saturation

V_{tn} - Threshold Voltage of NMOS Transistor

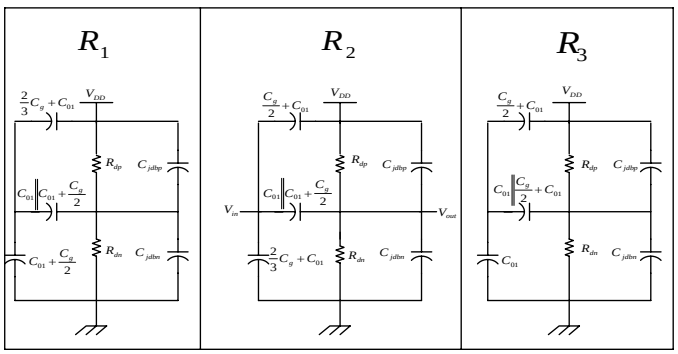
V_{tp} - Threshold Voltage of PMOS Transistor

After discussing transistor completely, the next step is modeling its 'RC' effects of CMOS Inverter in different regions of operation. The Resistance of transistor can be modeled over a range of time (t_1, t_2) [10]

$$R_{eq}\approx\frac{1}{2}\left[R_{dsp}(t_1)+R_{dsp}(t_2)\right] \quad (27)$$

$$=\frac{1}{2}\left[\frac{V_{dsp}(t_1)}{I_{dsp}(t_1)}+\frac{V_{dsp}(t_2)}{I_{dsp}(t_2)}\right] \quad (28)$$

TABLE IV
Equivalent RC Modeling of CMOS inverter



$$R_{eq} = R_{dsp} \;\&\; C_{eq} = \sum C \quad (29)$$

The equivalent resistance & Capacitance of the CMOS inverter are modeled in three different regions of operation during the interval $\left(t_1, t_{gr}+\frac{t_f}{2}\right)$, as given in Table IV [9]. Now the RC interconnect circuit is simplified as in Fig.11.

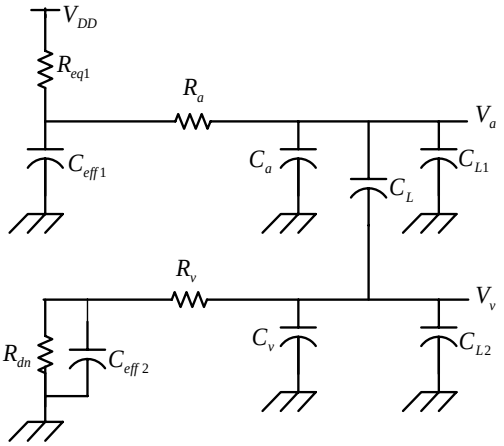


Fig.11. Simplified RC interconnect model of Transistor based circuit

The time constant due to each node is obtained by computing equivalent resistance seen across each capacitance, with all capacitances open circuited. The time constant at the node V_v is equal to as in [6]

$$\tau_v=R_{eq1}\left(C_{eq1}+C_1+C_C+C_{L1}\right)+R_1\left(C_1+C_C+C_{L1}\right)+\left(R_2+R_{eq2}\right)\left(C_C+C_{eff2}+C_2+C_{L2}\right) \quad (30)$$

The voltage at victim node is given by

$$V_V=V_{DD}\left(1-e^{\frac{-t}{\tau_v}}\right) \quad (31)$$

The above expression is much effective and accurate to estimate voltages at aggressor and victim nets in time domain. To compute peak value, this expression needs only time constant. Within one iteration, voltage at the victim net can be computed using (31) considering (30) as time constant. We demonstrate the accuracy of our model by conducting an experiment with the following 0.18µm technology specifications.

μ_n = 670 $cm^2/v-s$; C_{ox} =1.6 fF/cm^2

μ_p = 250 $cm^2/v-s$; E_{CNL} = 0.476 V;

V_{tn} = 0.2V; V_{tp} = -0.2V; E_{CPL} = 1.28V;

V_{sat} = $8\times10^6\,cm/s$; V_{DD} = 2.5V;

L = 0.25µm; W_{N1} = 5µm; W_{P1} = 10µm;

W_{N2} = 5µm; W_{P2} = 10µm;

The circuit behavior is modeled and tabulated in TABLE V.

TABLE V
Sample Experiment Data

	R_1	R_2	R_3
V_{in} (V)	2.3 0.8	0.8 0.2	0.2 0
V_g (mV)	50 0.19	0.19 0.71	0.71 1.49
V_V (mV)	19 80	80 279	279 420
I_{dsp} (μA)	117 420	420 908	908 655
R_{eq1} (KΩ)	13.43	5.02	31
C_{eff1} (fF)	46	620	185
t (ns)	0.37 0.68	0.68 1.00	1.00 1.68

$$V_V = V_{DD}(1-e^{\frac{-t}{\tau_{V1}}}) \qquad t_1 < t \le t_2$$

$$= V_{DD}(1-e^{\frac{-t}{\tau_{V2}}}) \qquad t_2 < t \le t_3$$

$$= V_{DD}(1-e^{\frac{-t}{\tau_{V3}}}) \qquad t_3 < t \le t_{gr} + \frac{t_f}{2}$$

$$= V_{Vpeak} e^{\frac{-t}{\tau_{V4}}} \qquad t > t_{gr} + \frac{t_f}{2} \quad (32)$$

V_{Vpeak} is the peak value at the far end node of victim net at $t = \frac{t_f}{2} + t_{gr}$. The time constants at different intervals τ_{V1}, τ_{V2}, τ_{V3} & τ_{V4} are computed using (30), by substituting the corresponding R&C values of Short Channel CMOS Inverter, from Table IV. Using (32), we can estimate the complete noise behavior in time domain. Fig.12 is the comparison of our metric with SPICE Simulation.

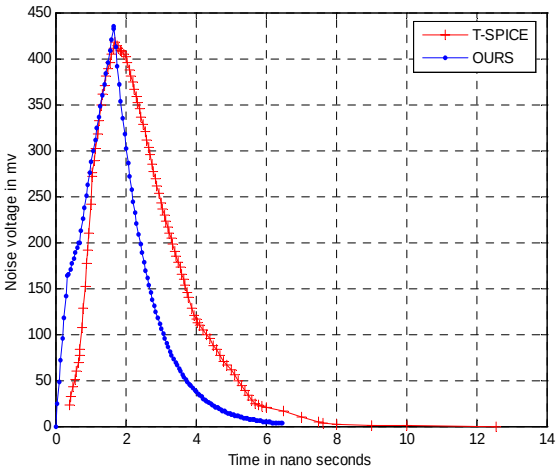


Fig.12 Comparison of Noise voltage between SPICE and our Metric

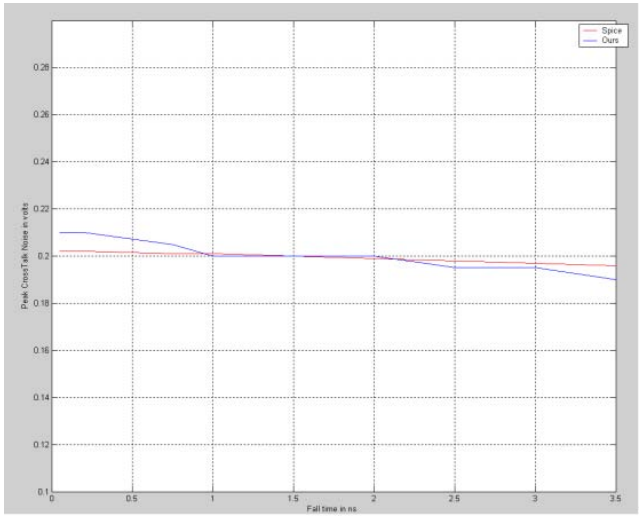


Fig.13 Effect of fall time on peak noise

Fig.13 shows variations of peak amplitude of crosstalk noise with respect to fall time of the ramp input, for a given set of line parasitics. We considered the first row data of Table VI and the fall time is varied from 0.1ns to 3.5ns. It is clear from the figure that our model is consistent and closely comparable with SPICE simulation. To prove the consistency of our metric, we performed an experiment on a two line CMOS inverter based RC interconnect circuit with SPICE simulation. The results are reported for a fall time of 1.0 ns with supply voltage of 2.5 V in generic 0.25μm CMOS technology. The widths of aggressor and victim inverters vary from 25μm to 5μm. Table VI contain the comparison between our metric and SPICE simulation. The computed propagation delay of CMOS inverter ranges between 0.5 ns to 1.00 ns. The mean and maximum errors are reported to be 5.3% and 17.4%, compared to SPICE simulation respectively.

TABLE.VI.
Results of Simulation on the two Capcitively Coupling Short Channel CMOS Inverter Based RC Interconnect model Using TSPICE and Our Metric.

P_1	N_1	N_2	R_a R_v KΩ/m	C_a fF/m	C_v fF/m	C_C fF/m	C_{L1} pf	C_{L2} pf	spice mV	OUR mV
40	20	20	28.5	300	300	400	0.82	0.5	420	439
40	40	40	28.5	300	300	400	0.82	0.5	248	265
80	40	40	28.5	300	300	400	0.82	0.5	358	368
80	20	20	28.5	300	300	400	0.82	0.5	566	599
80	20	40	28.5	300	300	400	0.82	0.5	361	376
40	20	40	28.5	300	300	400	0.82	0.5	235	276
40	40	20	28.5	300	300	400	0.82	0.5	392	405
80	80	80	28.5	300	300	400	0.82	0.5	221	228
100	40	40	28.5	300	300	400	0.82	0.5	409	415
100	40	80	28.5	300	300	400	0.82	0.5	258	248

E. Analytical Delay Models

We now develop analytical 50% delay model for RC interconnect using our proposed models (16) and (32). The 50% delay is defined as the time difference between 50% points of the input and far-end output of the aggressor net. Equating the aggressor far end voltage to $0.5V_{dd}$ in (16) and (32) and determine 't', which is denoted as t_a followed by

$$50\%Delay = t_r / 2 - t_a \tag{33}$$

Our proposed delay models for linear and non-linear driver are validated with different line parasitics as in Table VIIA & VIIB respectively. The maximum, minimum and mean estimation errors are

E. Analytical Energy Dissipation Model

Consider Fig.6, the source of energy dissipation in all the capacitors is V_{dd} through R_a, as the adjacent wire is quiet. Hence we find the energy dissipation in the low to high transition of the input source is [12] by

$$E^{L\to H} = \int_0^{T/2} \frac{[V_{dd} - V_a(t)]^2}{R_a} dt \tag{34}$$

In (34) the voltage drop across resistor can be computed by applying KVL in Fig.6 as follows.

$$V_{dd} - V_a(t) = e^{-t/\tau}.V_{dd} \tag{35}$$

The energy dissipation in all the capacitors through R_a over an interval of (0,T/2) is given by

$$E^{L\to H} = \frac{V_{dd}{}^2.\tau}{2R_a}\left[1 - e^{\frac{-T}{\tau}}\right] \tag{36}$$

Using (36), we can find the energy dissipation by all capacitors in linear and non-linear resistance based drivers for an interval (0, T), which are tabulated for different line parasitics in Table VIIA & VIIB. To take combined effect of delay and energy dissipation due to RC interconnect, we introduce a new performance metric, Energy-50% Delay Product (EDP). Fig.14 and Fig.15 show EDP per clock cycle of an RC interconnect with linear driver and non-linear driver respectively.

Table VIIA
Results of Delay and Energy dissipation due to RC interconnect with linear resistance as driver.

R1 KΩ/ m	*Rs1 Ω*	*R2 KΩ /m*	*Rs2 Ω*	*C1 pF/ m*	*C2 pF/ m*	*Cc pF/ m*	*Spice Delay ps*	*Our Delay ps*	*Our Energy fJ*
11	500	10	2500	60	64	100	43	52	72
9	75	10	150	92	80	170	65	80	366
17	325	17	335	140	100	200	242	267	100
12	190	8	100	85	75	140	285	298	144
9	527	9	400	72	72	150	75	85	67
8	270	7	240	83	90	160	50	63	130
10	625	10	750	120	120	132	161	174	57
15	800	15	550	108	108	200	353	366	44
13	270	20	250	130	100	220	169	156	124
9	26	15	550	97	30	120	34	36	978

Table VIIB
Results of Delay and Energy dissipation due to RC interconnect with non-linear resistance as driver.

Ra &Rv KΩ/ m	P1	N1	N2	C1 pF/ m	Cc pF/ m	Spice Delay ns	Our Delay ps	Our Energy fJ
11	40	20	20	300	400	0.98	0.93	44
9	40	40	40	300	400	0.5	0.49	85
17	80	40	40	300	400	0.52	0.5	83
12	80	20	20	300	400	1	0.95	42
9	80	20	40	300	400	1.01	0.88	45
8	40	20	40	300	400	0.99	0.93	45
10	40	40	20	300	400	0.5	0.54	88
15	80	80	80	300	400	0.33	0.27	164
13	100	40	40	300	400	0.57	0.49	86
9	100	40	80	300	400	0.58	0.47	88

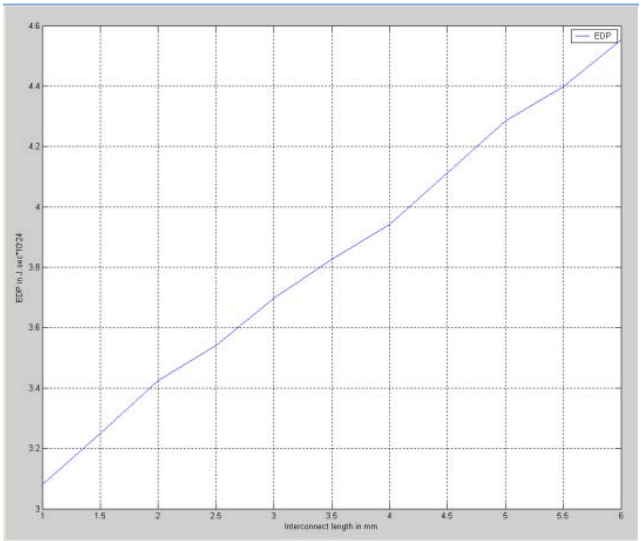


Fig.14 EDP in terms of line parasitics in an RC Interconnect with a linear driver.

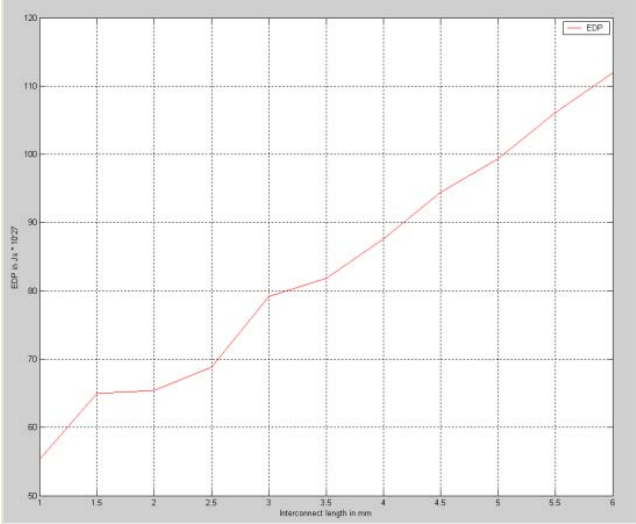


Fig.15 EDP in terms of line parasitics in an RC Interconnect with non-linear driver.

III. Conclusion

We proposed accurate closed form solutions to obtain Crosstalk Noise Voltage waveform in time domain for an RC interconnect in two cases. We addressed main drawbacks of Devgan's and Heydari's metrics, such as, adjustment to compute time constant of RC network and considering inaccurate value as steady state value using Devgan's metric in calculating peak amplitude of crosstalk. Further, our model reduces the computational overhead, as it takes one iteration to find peak amplitude of crosstalk noise at any node of aggressor and victim nets. Further we developed another model to handle non-linear resistance as the driver. We have considered the short channel effects of the CMOS transistors in this case. Results show that our metric captures the noise waveform shape well and yield an average estimation error of 3.366 % for noise peak over a wide range, in the linear driver case and 5.3% in the non-linear driver case. We applied our analytical models to derive analytical delay and energy estimation models. Finally, we conclude that our RC interconnect models are accurate, fast and real time solution for the signal integrity issue in complex wiring system.

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