VU Meter Driver Simulation and Design

Martin Pospisilik, Milan Adamek

***Abstract*—This paper deals with a design, construction and practical testing of a VU meter driver that includes an accurate rectifier and logarithmical driver of a pointer-type gauge. The logarithm is taken from the rectified signal by employing a capacitor discharge voltage curve. Several software simulations were made in order to proof the circuit design. Then a simple rectifier and logarithmiser was designed and built in order these simulations were proved and afterwards, based on the gained experience, the more complex design of the VU meter driver was created. The paper incorporates mathematical description of the circuit, simulation results and results gained when the simple driver circuit underwent several physical tests as well as further propositions for practical extensions of the designed circuit.**

***Keywords*—**Hardware logarithm processing, VU meter, audio signal rectifier, gauge driver

I. Introduction

ANALOG audio signal levels are often expressed in decibels compared to one reference level. Analogous VU meters are usually equipped with a non-linear decibel scale which stem from the definition of a ratio unit [dB]. In this case only a simple front end rectifier is sufficient for a satisfactory level indication. However, it is more comfortable to take and display directly the logarithm of the voltage level of the signal because then we gain an advance of a linear gauge scale. In addition, the gauge range is usually extended to at least 30 dB.

There are several requirements that should be met by the accurate VU meter:

- Symmetrical processing of the AC signal voltage with low distortion observing the sufficient bandwidth,
- accurate measuring of the peak value (in audio systems there is usually a need to display peak values to prevent the signal from clipping the peaks),
- the peak value should be displayed for a period of time that is long enough so the user could clearly see it on the scale,
- the reaction time of the VU meter should be short enough so very short peaks could be displayed,
- it is convenient to take and display the logarithm of the measured value because of the typical character of the audio signal.

To meet these requirements, the advanced rectifier and driver for analog VU meter was designed and built. When designed, many simulations were processed with the aid of Multisim software. The performance of the built circuit was physically tested and the results achieved were comparable to the results of the simulations. Based on this experience a more complex 2-channel VU meter driver was designed and built. Primarily, this circuit was designed to be used in a vacuum valve amplifier as a power indicator. Therefore, several initial conditions may seem to be quite unusual, for example the power supply voltage of 6.3 V. However, the main principle can be applied to a wider variety of applications.

II. Logarithmical PWM Modulation

The basic aim was to employ a quite simple method of processing a pulse-width modulation by a comparator-connected operating amplifier. The voltage the logarithm is taken of is periodically compared to a reference voltage that can be described by the following equation:

$$u_{REF} = U_0 \cdot e^{-\frac{t-nT_0}{\tau}}; \quad t \in \langle 0, T_0); n \in N \tag{1}$$

Where:

- U_0 is the amplitude of the reference voltage [V],
- t is time flowing throughout the period T_0 [s],
- T_0 is a period of pulse width modulation [s],
- n is the order of the appropriate period [-],
- τ is a time constant defining the voltage slope [s].

To get the best resolution we need to obtain the highest possible amplitude of the reference voltage. Ideally, u_{REF} lies in the range between $U_0 = U_{cc}$ at t = 0 and 0 at $t = T_0$. Practically, we will let the voltage to drop to 10 % of U_0 which can be well implemented physically. Considering this level must be achieved in a period of T_0, we can determine the optimal value of τ:

$$0.1 \cdot U = U_0 \cdot e^{-\frac{T_0}{\tau}} \Rightarrow \tau = -\frac{T_0}{\ln(0.1)} \tag{2}$$

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The behavior of the signal is described in Fig 1. with a curve called "Modulator reference voltage" as a result of computer simulations applied to the circuit the design of which is described in this paper. One can see that the slope of the voltage is exponential. Comparing this voltage to a direct voltage of a random level at the input of the modulator, the output of the modulator can be described with the following equation:

$$u_{OUT} = \begin{cases} 0 \Leftrightarrow u_{IN} < u_{REF} \\ U_{CC} \Leftrightarrow u_{IN} \geq u_{REF} \end{cases} \quad (3)$$

Where:

- u_{OUT} is the output voltage of the ideal modulator [V],
- u_{IN} is the input voltage of the modulator [V],
- U_{cc} is the supply voltage of the ideal modulator [V],
- u_{REF} is the reference voltage of the modulator described by equation (1) [V].

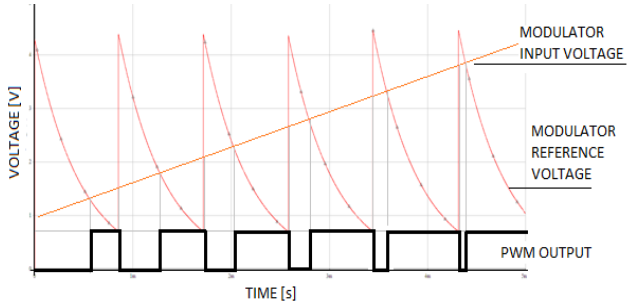

Fig. 1 Modulator signals (simulation results)

Considering a period of pulse width modulation T_0 [s] and a period of time when the output of the modulator is in a high state ($u_{OUT} = U_{cc}$) t_H [s], the ratio of the output signal of the modulator R can be simply described as:

$$R = \frac{t_H}{T_0} \quad (4)$$

In order to determine the value of R we must find such time t throughout the period of T_0 in which $u_{IN} = u_{REF}$, because at this point lies the threshold of the comparator. Provided we consider invariable direct voltage at the input of the modulator, we can describe the dependence of R on u_{IN} (using equations 1, 2, 3, 4) as:

$$u_{IN} = const. = u_{REF} = U_0 \cdot e^{-\frac{t-nT_0}{\tau}} \quad (5)$$

$$t = -\frac{T_0}{\ln 0.1} \cdot \ln\left(\frac{u_{IN}}{U_0}\right); \quad R = \frac{t}{T_0} \quad (6)$$

$$R = -\frac{1}{\ln 0.1} \cdot \ln\left(\frac{u_{IN}}{U_0}\right) \quad (7)$$

From the equation (7) we can see the logarithmic dependence of R on the input voltage u_{IN}. Because the level of signal in [dB] is defined as Briggsian logarithm of the ratio between the measured and the reference level and the modulator, as deduced above, makes the Napierian logarithm, we need to recalculate the output of the modulator so as to order the proper scale was achieved. According to [1] we can use simple approximation:

$$\log x \approx 0.434\,294 \cdot \ln x \quad (8)$$

The behavior of a PWM modulator with a reference voltage according to (1) can be seen in Fig. 1. There are two input voltages (modulator input voltage and modulator reference voltage) and the appropriate output of the modulator displayed.

At the output of the modulator we get two-state signal with the ratio R. Throughout the period T_0 this signal can be expressed with the aid of the Heaviside step function:

$$u_{OUT} = U_{CC} \cdot H\left(t - (1-R) \cdot T_0\right); \quad t \in \langle 0, T_0 \rangle \quad (9)$$

Integrating this signal in time, we get direct voltage corresponding to R. We can express the mean value with the successive equation:

$$\begin{aligned} U_{MEAN} &= \frac{1}{T_0}\int_0^{T_0} u_{OUT}\, dt \\ &= \frac{1}{T_0}\int_0^{T_0} U_{CC} \cdot H\left(t - (1-R)\cdot T_0\right) dt \\ &= \frac{1}{T_0} \cdot \left(\int_0^{(1-R)T_0} 0\, dt + \int_{(1-R)T_0}^{T_0} U_{CC}\, dt \right) \\ &= \frac{1}{T_0} \cdot \left([0 \cdot t]_0^{(1-R)T_0} + [U_{CC} \cdot t]_{(1-R)T_0}^{T_0} \right) \\ &= \frac{1}{T_0} \cdot \left(T_0 \cdot U_{CC} - (1-R) \cdot T_0 \cdot U_{CC} \right) = R \cdot U_{CC} \end{aligned} \quad (10)$$

III. CIRCUIT DESCRIPTION

The circuit was built on a single-layer PCB. A high emphasis was placed on ease of the construction and low cost of the components. Before the description of the practical construction is provided, let us shortly see how the circuit can be particularized into several logical blocks.

A. Logical blocks of the circuit

The circuit can be particularized into several blocks that can be seen in Fig. 2. At the input of the circuit, there is an input

buffer that accommodates this circuit to preceding circuits in terms of the voltage level and the impedance of the signal. As there are two rectifiers employed in the circuit in order to improve the symmetry of either positive or the negative half-wave of the signal, one of the rectifiers must be front-ended with an inverter. Outputs of both rectifiers are then summarized by an analog summer and a simple peak memory. These blocks are simply based on a larger capacitor. The differentiator derivates the voltage on the peak memory capacitor in time and when a steep voltage peak occurs, it generates a short pulse that is added to the voltage on the memory capacitor. This improves the response of the pointer of the gauge as it is pushed by a high current pulse. The proper response of the differentiator must be identified by a practical experiment with an appropriate gauge so the pointer does not overshoot the proper position. Now we come to the modulator which is based on a comparator that processes two signals – the voltage of the peak memory capacitor with a short pulse eventually added by the differentiator and the exponential voltage decay generated by a non-reciprocal RC integrator according to equation (1). The oscillator generates periodic pulses that are used to charge the integrator capacitor very fast while the discharge of the capacitor is executed slowly. The output buffer integrates the output voltage according to equation (10) and drives the scale.

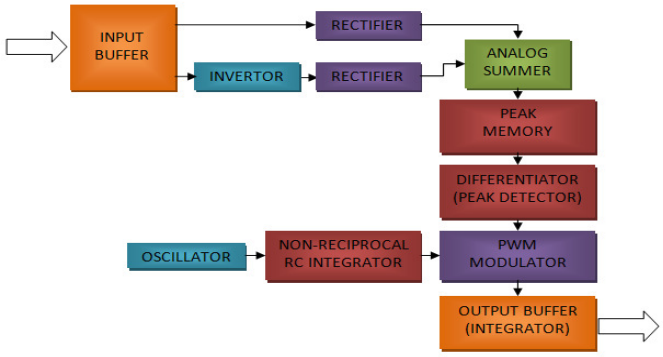

Fig. 2 Circuit block diagram

B. *Detailed description*

The schematics of the circuit can be seen in Fig. 3. There are three pin terminals in the circuit. These terminals are marked SL1 to SL3. SL1 serves to connect the power supply of 6.3 V. The pointer-type gauge is connected to SL3 and at SL2 there is the input of the driver. The aim was to make the circuit as simple as possible. This is the reason why only three transistors and two integrated circuits are employed in the schematics. Let us closely describe individual functional blocks of the circuit.

1. *Input buffer and invertor*

The input buffer and the inverter are both implemented by T2 transistor. Its operating point is set by resistors R2 and R7. Their values were set according to simulation of the circuit so the output amplitudes of the inverted and non-inverted outputs were clipped at equal levels – an optimal bias was found to be set at approx. 40 % of the supply voltage. The bias voltage is blocked by the capacitor C3. The level of the input signal can be adjusted by the rotary trimming resistor R17. The values of R17 and boundary resistors R10 and R26 were determined considering the circuit to be connected to the output of 100 W audio amplifier. The signal level behind the trimming resistor R17 is supposed to be around 0.3 V_{ef} for the pointer displacement of 0 dB (80 % of the whole scale). The quiescent current through the transistor T2 is supposed to be around 450 µA. At the collector of T2 we get the signal with 180° phase shift while at the emitter of the same transistor we get the signal with no phase shift. Collector and emitter resistors R5 and R27 are of equal value so the transistor works with a negative feedback of 100 %. Provided the outputs of input buffer / inverter are loaded with high impedance, the signal amplitudes at both outputs should be almost identical.

2. *Rectifiers and peak memory capacitor*

There are two rectifiers in the circuit, based on operating amplifiers IC2A and IC2B. This is to improve the symmetry of the rectifier at high frequencies at which reverse recovery times of the diodes and limited slew rate of the operating amplifiers may take effect. The circuit was a subject of software simulations together with the input buffer and inverter

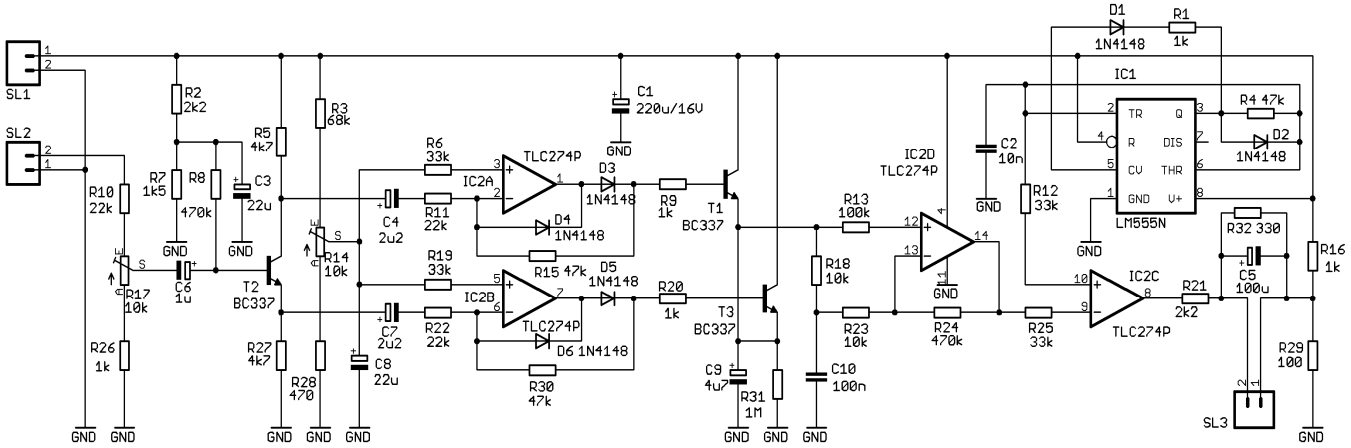

Fig. 3 Detailed circuit diagram

and analogous summer and the results acknowledged better linearity of AC to peak DC conversion at high frequencies and low amplitudes. Decoupling of rectifier inputs is realized with the aid of C4 and C7 capacitors. Each of both operating amplifiers is connected in the way of inverting amplifier for a negative half-wave with a gain of approximately 6 dB while for the positive half-waves the outputs of operating amplifiers are blocked by D3 and D5 diodes and their negative feedback is ensured by D4 and D6 diodes so the amplifiers are protected from deep negative saturation. The outputs of these operating amplifiers are fortified by T1 and T3 transistors that deliver the sufficient amount of current to charge the memory capacitor C9 to the proper peak value in a short time. Practically, some low bias is needed to set the optimal working points of the operating amplifiers and transistors. This bias is set by the rotary trimming resistor R14 in such a way that the quiescent voltage at C9 capacitor lies between 0.25 and 0.4 V. Successive blocks like differentiator and PWM modulator also take advantage of this bias. The outer effect of setting the bias is that the pointer of the gauge remains at the bottom of the scale when the driver is not excited. The value of the peak memory capacitor C9 is selected in order to ensure the charging time is fast enough while the discharge takes approximately 7.5 s.

3. Differentiator

The differentiator is based on the IC2D operating amplifier. At first glance it seems it is connected similarly to the differential amplifier. Considering just the IC2D operating amplifier with resistors R13, R23 and R24 and that there are two inputs of the circuit, IN^+ and IN^-, both on the sides of the resistor R18, which is for our purposes omitted now, its output voltage can be loosely expressed like:

$$U_{OUT_{IC2D}} \cong U_{IN}^{+}\left(\frac{R_{24}+R_{23}}{R_{23}}\right)-U_{IN}^{-}\frac{R_{24}}{R_{23}} \tag{11}$$

Neglecting the influence of the resistors R13 and R18 and the capacitor C10, we find $U_{IN}^+ = U_{IN}^- = U_{IN}$. Thus, the amplification of the circuit can be expressed like:

$$A \cong \frac{U_{OUT_{IC2D}}}{U_{IN}} \cong \frac{R_{24}+R_{23}}{R_{23}}-\frac{R_{24}}{R_{23}}=\frac{R_{23}}{R_{23}}=1 \tag{12}$$

Therefore, it is possible to state that for signals that change their voltage slow enough so there is no delay produced by the derivative element made of the resistor R18 and the capacitor C10, the amplification factor is close to 1. On the other hand, if we suppose that the voltage at the input of the differentiator changed at a single jump from the value U_0 to U_{PEAK}, the voltages U_{IN}^+ and U_{IN}^- that can be found on both ends of the resistor R18, can be then, when neglecting influences of other circuit parts, expressed like:

$$u_{IN}^{+} = U_0 + (U_{PEAK}-U_0)\cdot H(t) \tag{13}$$

$$u_{IN}^{-} = U_0 + (U_{PEAK}-U_0)\cdot\left(1-e^{-\frac{t}{R_{18}C_{10}}}\right)\cdot H(t) \tag{14}$$

Based on this simplification, the reaction of the differentiator output to this jump can be estimated like:

$$\begin{aligned} u_{OUT_{IC2D}} \cong & \left(U_0+(U_{PEAK}-U_0)\cdot H(t)\right)\cdot\left(\frac{R_{24}+R_{23}}{R_{23}}\right) \\ & -\left(U_0+(U_{PEAK}-U_0)\cdot\left(1-e^{-\frac{t}{R_{18}C_{10}}}\right)\cdot H(t)\right)\cdot\frac{R_{24}}{R_{23}} \end{aligned} \tag{15}$$

In a very short time after the voltage jump ($t \ll R_{18}C_{10}$) we can contemplate the voltage on the capacitor C10 is still U_0, thus:

$$\begin{aligned} u_{OUT_{IC2D}} &\cong U_{PEAK}\cdot\frac{R_{24}+R_{23}}{R_{23}}-U_0\cdot\frac{R_{24}}{R_{23}} \\ &= 48\cdot U_{PEAK}-47\cdot U_0 \end{aligned} \tag{16}$$

The short time amplifying factor can be expressed as a ratio of the output voltage to the "quiescent" voltage U_0:

$$A_{IC2D_{PEAK}} = \frac{U_{OUT_{IC2D}}}{U_0} \cong 48\cdot\frac{U_{PEAK}}{U_0}-47 \tag{17}$$

The higher the voltage jump is the higher is its amplification, which corresponds well to the requirement that short and steep pulses must be amplified enough so the gauge could react properly on them. In reality, steep pulses drive the differentiator to the positive saturation which causes driving the PWM modulator to the highest possible R ratio. With respect to Nyquist-Shannon sampling theorem, if the positive pulse at the output of the differentiator lasts enough time, we get a voltage pulse at the output of the circuit that forces the pointer of the gauge.

4. PWM modulator, reference signal generator and the output buffer

PWM modulator is in fact very simple, consisting of the operating amplifier IC2C that compares the voltage at the output of the differentiator to the reference voltage. The principle of this operation has been described above. The reference voltage is generated right on the timing capacitor C2 that defines how the timer IC1 will oscillate as an astable circuit. Imagine that at the moment the driver is being turned on the capacitor C2 is discharged. TRIGGER voltage input (pin 2) of the timer IC1 is lower than the trigger value and therefore the output of the timer (pin 3) will reach level H. The capacitor C2 is now rapidly charged through the diode D2. When its voltage exceeds ⅔ of the supply voltage, the THRESHOLD input of the timer (pin 6) will cause flipping the timer to the low output level. Now, the capacitor C2 discharges through the resistor R4. Because the CV input of the timer (pin 5) is now tied low to the timer output (pin 3) by the help of the diode D1 and the resistor R1, the voltage on the capacitor C2 must drop lower than to ⅓ of the supply voltage

so the input TRIGGER drove the output of the timer high, leading to generate quasi-logarithmical voltage decay. It is not crucial how stable the capacity of the capacitor C2 is because its change affects only the period T_0, not the shape of the signal. The shape can be affected by leakage current through the capacitor and the inputs of the connected integrated circuits but in this case these influences can be neglected. The output buffer consists of the resistors R21, R32 and the capacitor C5. The values of R32 and C5 were found by practical tests with the particular gauge. They both damp overshoots of the pointer down. A voltage divider made of resistors R16 and R29 serves to bias the gauge so the influence of the bias set by the trimming resistor R14 is neutralized.

5. *List of parts*

Below there are lists of parts the circuit was made of.

Table 1 Resistors

Part number	Value	Specification
R1, R9, R16, R20, R26	1kΩ	RM0207, metal oxide, 0.5 W
R2, R21	2,2kΩ	RM0207, metal oxide, 0.5 W
R3	68kΩ	RM0207, metal oxide, 0.5 W
R4, R15, R30	47kΩ	RM0207, metal oxide, 0.5 W
R5, R27	4,7kΩ	RM0207, metal oxide, 0.5 W
R6, R12, R19, R25	33kΩ	RM0207, metal oxide, 0.5 W
R7	1,5kΩ	RM0207, metal oxide, 0.5 W
R8, R24	470kΩ	RM0207, metal oxide, 0.5 W
R10, R11, R22	22kΩ	RM0207, metal oxide, 0.5 W
R13	100kΩ	RM0207, metal oxide, 0.5 W
R14, R17	10kΩ	Rotary trimming resistor PT10-L (gridr 5x10mm, horizontal)
R18, R23	10kΩ	RM0207, metal oxide, 0.5 W
R28	470Ω	RM0207, metal oxide, 0.5 W
R29	100Ω	RM0207, metal oxide, 0.5 W
R31	1MΩ	RM0207, metal oxide, 0.5 W
R32	330Ω	RM0207, metal oxide, 0.5 W

Table 2 Capacitors

Part number	Value	Specification
C1	220μF	Electrolytic, radial, grid 5mm, ∅ 5mm, > 10 V
C2	10nF	Ceramic, tolerance ± 20 %
C3, C8	22μF	Electrolytic, radial, grid 5mm, ∅ 5mm, > 10 V
C4, C7	2,2μF	Electrolytic, radial, grid 5mm, ∅ 5mm, > 10 V
C5	100μF	Electrolytic, radial, grid 2mm, ∅ 5mm, > 10 V
C6	1μF	Electrolytic, radial, grid 5mm, ∅ 5mm, > 10 V
C9	4,7μF	Electrolytic, radial, grid 5mm, ∅ 5mm, > 10 V
C10	100nF	Ceramic, tolerance ± 20 %

Table 3 Semiconductors

Part number	Value	Specification
D1, D2, D3, D4, D5, D6	1N4148	General diode with low t_{rr}
IC1	LM555N	Or equivalent
IC2	TLC274P	OA for low-voltage applications
T1, T2, T3	BC337	General NPN transistors

Table 4 Other

SL1, SL2, SL3	Connectors, grid 2,54mm
Analogous gauge	R_i = 600Ω, I_m = 500μA

6. *PCB layout*

The circuit was built on a single-layer PCB 90 x 60 mm. The layouts of the PCB are shown below.

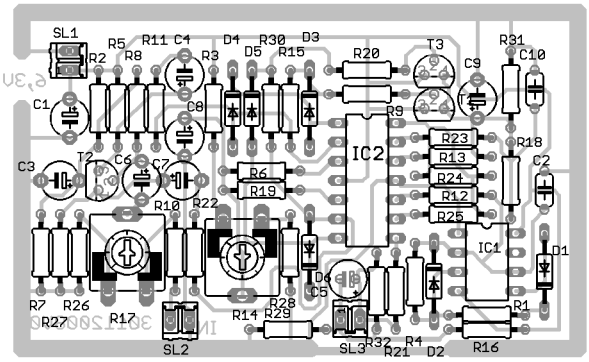

Fig. 4 Circuit parts displacement

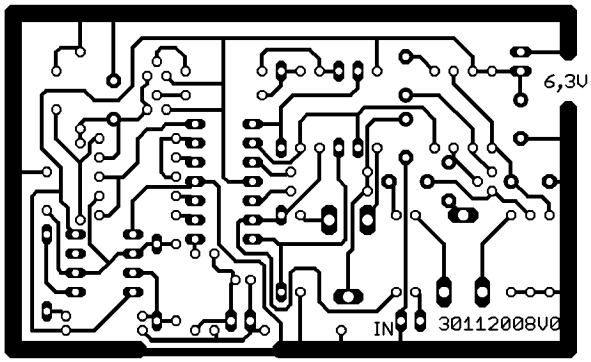

Fig. 5 PCB layout (bottom)

IV. Results

The above described circuit was built and underwent several tests the results of which are discussed below. The pointer-type gauge according to specification in Tab. 4 was connected and the circuit was supplied with 6.3 V (as acknowledged above). The air temperature was 20 °C. The input of the circuit was driven by an accurate programmable function generator. The sensitivity was set by the resistor R17 so that at 1 V_{RMS} @ 1 kHz sinusoidal signal the pointer of the gauge stayed at 80 % of the scale (at this point typically 0 dB mark occurs on the scales). The bias was set by the resistor R14 so that pointer indicated 0 % of the scale when no signal was fed into the circuit input.

A. *Rectifier frequency response*

The frequency of the sinusoidal signal was changed from 1 Hz to 500 kHz at 1 V_{RMS} and the corresponding voltage was measured by a digital voltmeter at the output of the operating amplifier IC2D (in front of the PWM modulator). Output signal level was expressed in dB compared to the level of the input signal and the results were plotted on the Fig. 6.

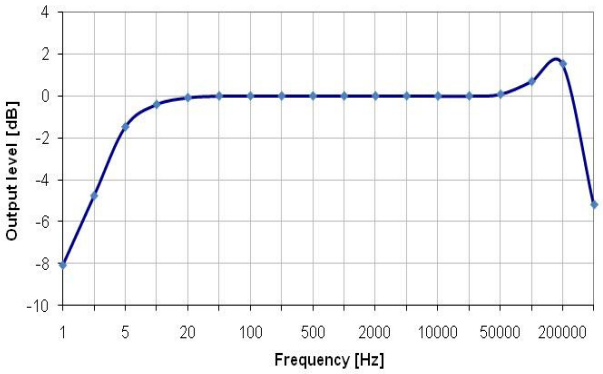

Fig.6 Rectifier frequency response

In the Fig. 6 we can see that for audible frequencies the output voltage of the rectifier is not influenced. The peak at the frequency of approximately 150 kHz is probably caused by effects of recovery of the diodes D3 – D6. If critical, the peak can be eliminated for example by connecting a 1 nF capacitor between the collector and the emitter of the transistor T2, which will not affect the circuit performance in any other aspects.

B. Logarithm processing

In this step it was tested how accurate is the logarithm taken from the rectified signal by the logarithmical PWM modulator. The input of the circuit was fed by sinusoidal signal at the frequency of 1 kHz. An RMS voltage was measured at the clamps of the analogous gauge by a digital oscilloscope so that the non-linearity of the gauge was extruded. The results were plotted into a diagram to be seen in Fig. 8. As a nominal value of 0 dB, the level of 1.55 V_{RMS} was set and the input voltage was changed from 0.15 V (- 20 dB) to 3.1 V (+ 6 dB). The input voltage is shown at the x-axis while at the y-axis there we can see the output voltage measured at the analogous gauge clamps.

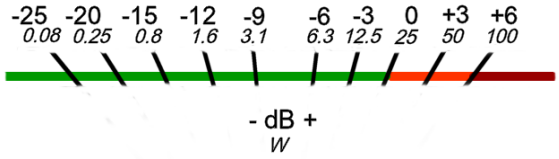

Fig. 7 An example of the scale that would be applicable to the gauge driven by the advanced VU meter driver. The scale is stamped in decibels and watts.

There are two curves in the diagram. The proper Briggsian logarithm is represented by the green line while the output of the logarithmic PWM modulator is represented by the blue line. As can be seen, at high levels both curves are almost identical while at low levels the blue curve becomes quite linear although the difference from the proper logarithm is, if the linearity of the analogous gauge is taken into account, quite acceptable.

What the scale would look like on the appropriate gauge can be seen in Fig. 8. It is presumable that the error at low levels is caused by the low voltage range of the reference signal as the supply voltage is quite low and the reference voltage falls under the value the operating amplifier IC2C can process properly.

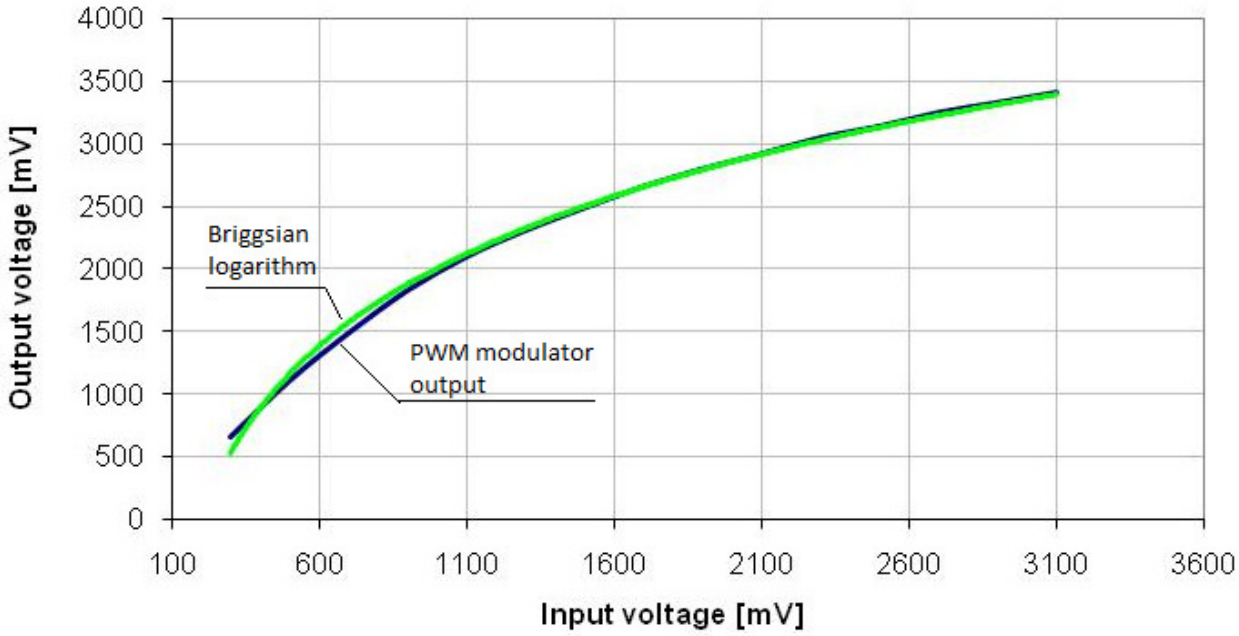

Fig. 8 Logarithmiser performance (measured)

C. Checking the differentiator

To check the proper function of the differentiator, the input of the driver was fed with short pulses with a period of 1 s. In Fig. 9 there is an oscillogram showing what the signal looked like in front of the differentiator (lower curve) and what it looked like behind the differentiator (at the output of the operating amplifier IC2D – the upper curve).

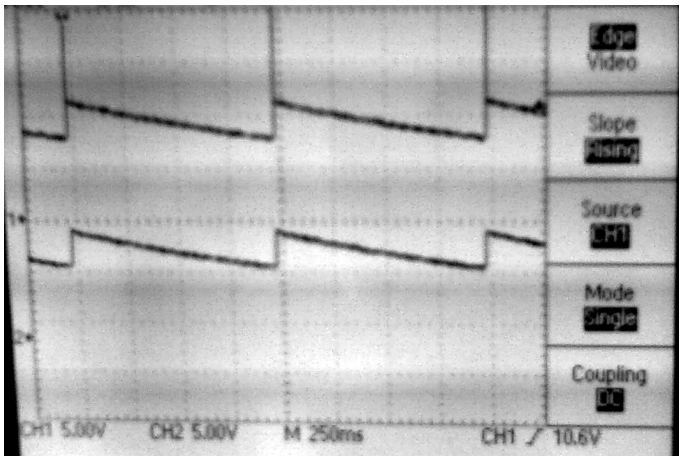

Fig. 9 Differentiator performance (measured). The lower curve represents the signal at the differentiator input while the upper curve represents the signal at the differentiator output

As stated above, steep pulses drive the differentiator to the positive saturation. The width of the pulse should be higher than 3 periods of the modulator reference signal.

In this particular case, the frequency of the reference signal was approximately 1.2 kHz (measured at the run of the circuit) so the pulses must last at least 2.5 ms. The duration of the pulses can be adjusted by the resistor R18.

V. Contemporary Development

Based on the positive experience gained by practical tests on the circuit shown in Fig. 3, more complex rectifier and driver has been designed for practical usage. Its circuit diagram can be seen in Fig. 10. The circuit is 2-channel with the inputs at the connectors SL1 and SL3. Analog VU meters are to be connected to the connector SL2. The circuit can be supplied with 6 V AC current, because it is supposed to be utilized in a vacuum-tube amplifier. The power supply is connected to the clamps X1 and a simple multiplier made of capacitors and diodes boosts the voltage to approximately 30 V. Then the parametric voltage regulator VR1 stabilises the voltage to 26 V. Increasing the supply voltage helps us to produce smoother and more accurate reference signal (see Fig. 1).

The construction of the input buffer and the rectifiers stayed unchanged, as well as the memory capacitor excitation. The 555 timer has been replaced with the operational amplifier IC1A that is connected as astable trigger circuit. According to simulations this trigger circuit should run at 280 Hz. The quasi-logarithmic reference signal is generated at the capacitor C6. The comparators made with the operational amplifiers IC2A and IC2D share it. Another approach was employed at

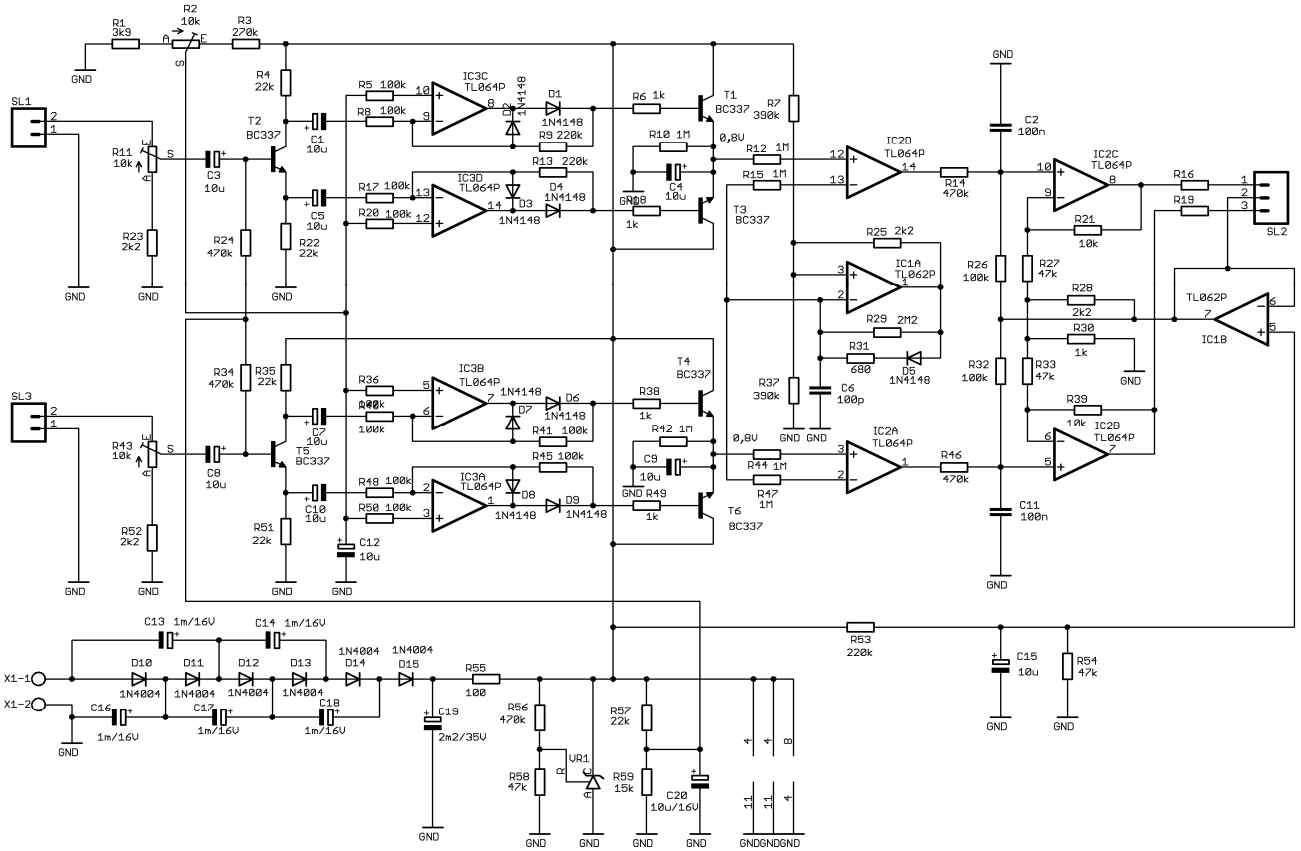

Fig. 10 Complex two-channel VU meters driver

gauge peak reaction. At the output of the PWM modulators there are integrators R14/C2 and R46/C11. The gauges are excited via the operational amplifiers IC2C and IC2B. The values of the resistors R16 and R19 should be as low as possible. Then the gauge systems are damped heavily because of the low output impedance of the operational amplifiers with the appropriate feedback loops. The operational amplifier IC1B delivers bias voltage to the gauges. The bias of both channels is to be set by the rotary trimming resistor R2.

At the present time this circuit is a subject to debugging.

A. Simulations

Because the input buffers, rectifiers and memory capacitors remained unchanged, no more simulations were made on these subcircuits. The function of the astable trigger circuit was proved with Multisim software as well as the function of the pointer gauges driver.

B. Mechanical construction

The sample of the complex driver was built on a single-layer printed circuit board the dimensions of which were approximately 140 x 80 mm. Only cheap and conventional devices were used, there is no need for special or expensive parts. The layout of the PCB can be seen in the figures below.

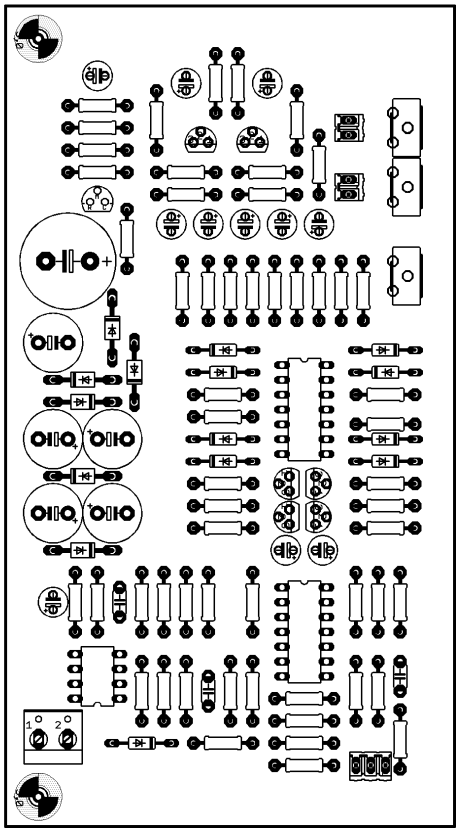

Fig. 11 Complex VU meter driver parts displacement

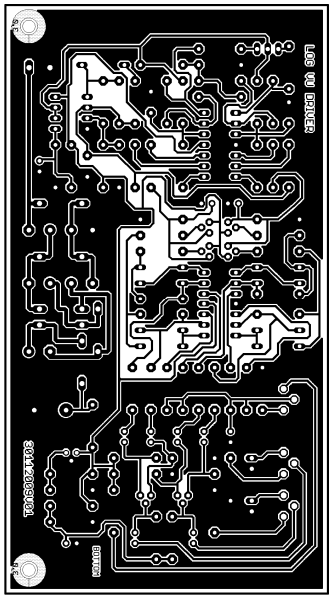

Fig. 12 Complex VU meter PCB layout

VI. CONCLUSION

In this paper a design of the hardware signal logarithmiser and VU meter driver is described. According to the theory mentioned at the beginning of the paper a simple VU meter driver was designed and built according to the simulations that were processed by Multisim software simulator. The results of physical measurements made on this circuit are also described in the paper. Finally, based on the gained experience, a complex two-channel logarithmising VU meter driver was designed and built.

The main advantages of the proposed construction are as follows: symmetrical proceeding of the input signal, almost ideal frequency response at audible frequencies, logarithmical voltage output and improved gauge response at steep pulses.

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