# Design and Evaluation of Hysteresial Threshold Gate based on Neuron MOS

Mototsune Nakahodo, Chikatoshi Yamada, Yasunori Nagata

***Abstract*— In this article threshold gates with hysteresis using neuron MOS ($\nu$MOS) are presented as basic elements in Null Convention Logic (NCL) circuits. NCL, which proposed by K. M. Fant and S. A. Branst, needs special gates having hysteresis, because NCL uses different ternary logic systems in computation phase and wiping phase of asynchronous behavior, respectively. To implement the dynamic behavior, the traditional NCL circuits exploit extended CMOS structure which consists of a number of cascaded and parallel transistors connections. Then we improve the circuits with the characteristics of threshold function in $\nu$MOS, we designed hysteresial $\nu$MOS by means of feedback loop. This results the asynchronous circuits reducing the number of MOS and wire area. We provide two synthesis methods and simulation results of the gates and full-adder. The evaluation results of area dissipation and average delay show the advantages of the proposed circuitry.**

***Keywords*— Asynchronous Circuit, Delay Insensitive, Neuron MOS, Threshold Gate**

## I. Introduction

HIGH-SPEED and high-performance synchronous circuit design in VLSI suffer some serious problems such as clock skew, clock noise and larger power dissipation. Asynchronous circuits solves such problems by use of request/acknowledge signaling instead of global clock direction. In the asynchronous circuit design, there are two main design categories based on. They are called bounded-delay model and self-timed model which came different assumption of delays [1].

In this article, quasi-delay-insensitive model (QDI), which is one of the self-timed model, is assumed [2]-[4]. The QDI model is currently most practical assumption to construct asynchronous circuit systems, that is, delays in both gate-elements and wires are unbounded, and additionally signals propagating through forked wire are arrive simultaneously to different destinations. On the other hand, Null Convention Logic (NCL [5]) is a technique for design of asynchronous circuits and satisfies QDI assumption. While QDI oriented circuits are unaffected by changing of delays, it requires over head circuitry.

We present threshold gate with hysteresis using $\nu$MOS as components of NCL circuit. Exploiting the $\nu$MOS can reduce numbers of MOS transistors, thus it will save total area enough to develop speed of circuits.

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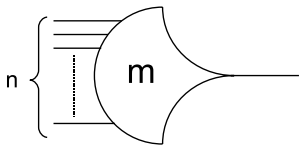


Fig. 1. Symbol of TH gate

## II. Two Phase System and NCL

### A. Overview of NCL

NCL offers a self-timed logic paradigm where control is inherent with each datum. And NCL paradigm assumes that forks in wires are isochronic [4]. The origins of various aspects of the paradigm, including the NULL logic state can be traced back to Muller's work on speed-independent circuits [6].

### B. Two Phase Data Transfer

Asynchronous circuit usually adopts dual-rail logic circuit to satisfy QDI assumption. NCL also assumes QDI and dual-rail structure. The behavior of dual-railed asynchronous circuits is called two phase data transfer for detecting data arrival. That is to say, initial state of circuit takes invalid data value (0 0) at inputs and output of element. This state is achieved wiping phase preceding computation phase. Thus dual-rail, refer table I, can transfer valid data and completion timing at a time. On the other hand, although this class of asynchronous circuits are usually based on weak Kleene logic (B-ternary logic [7]), NCL exploits strong Kleene (C type logic [8]) in computation phase and weak Kleene in wiping phase. To achieve this interesting system behavior, circuit requires hysteresis gates to justify front of wave of computations.

### C. Threshold gate with hysteresis

Threshold gate with hysteresis (TH gate) is used in order to synthesis of NCL circuits [10]. Fig.1 is a symbol of TH gate.

TABLE I
DUAL-RAIL TERNARY DATA EXPRESSION

| $D_1$ | $D_0$ | contents |
|---|---|---|
| 0 | 0 | invalid (NULL) |
| 0 | 1 | valid data 0 |
| 1 | 0 | valid data 1 |

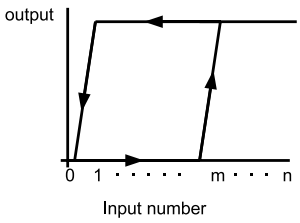


Fig. 2. Wave of THmn

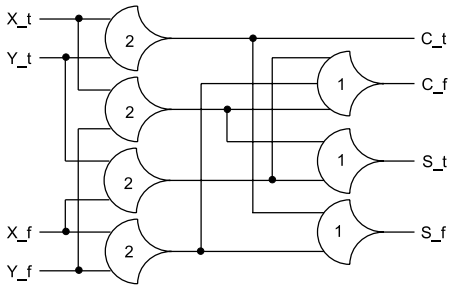


Fig. 3. NCL Half Adder

TH gate has two parameters, one is the number of inputs and the other is a threshold value. A hysterisial threshold gate which has n-inputs and threshold n is described as THmn hence force. Fig.2 is wave of THmn. Note that the threshold m means that the gate output is activated to ON when m inputs or more are activated. Afterward output retains ON while all of input deactivated to OFF. In other words, TH gate is a special gate such as threshold of activating and deactivating are different. Note that a THmn has activating threshold m and deactivating threshold 1, thus the output has hysteresis.

NCL circuit which has TH gate can synthesize. Fig.3 is NCL half adder. It can synthesize register and control circuit as well as combinational circuit [9].

Fig.4 shows a TH gate synthesis using MOS transistors. It is called *block type* TH gate because it has four MOS network blocks. For instance, Fig.5 is a block type TH23 gate. Block type requires a number of MOS transistors.

## III. Design of TH gate using $\nu$MOS

### A. Basis of $\nu$MOS

$\nu$MOS (neuron MOS) is one of the floating gate which has some inputs and an output. Fig.6 is the structure of $\nu$MOS and fig.7 is the equivalent circuit. The behavior of $\nu$MOS is as follows. Suppose $V_0$=0 as in fig.7 and the $V_F$ in the floating gate is stated as follows.

$$V_F = \frac{\sum_{i=1}^{n} C_i V_i}{\sum_{i=0}^{n} C_i} \tag{1}$$

That is, $V_F$ increases depending on the number of asserted inputs $m'$. When threshold voltage is $V_{th}$ and $C = C_1 = C_2 = \cdots = C_n$, the ON condition of $\nu$MOS is stated as follows.

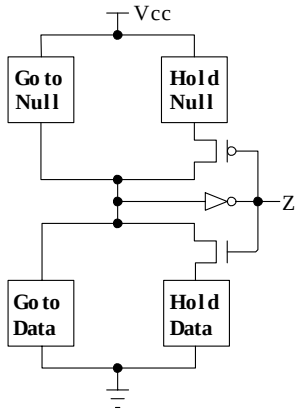


Fig. 4. Block type TH gate

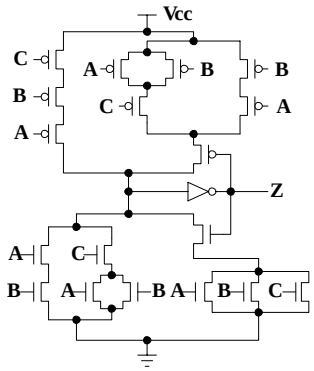


Fig. 5. Block type TH23

$$V_F = m' \cdot \frac{C}{nC + C_0} V_d > v_{th} \tag{2}$$

where $C_0$ is the capacitive coupling coefficient between the floating gate and the substrate. Therefore, when the number of activated inputs m' exceeds threshold m, the $\nu$MOS activate to ON.

Fig.8 is a $\nu$MOS threshold gate having three inputs. The output of the gate is activated when two or more inputs are activated.

In the following we propose two kinds of techniques to implement TH gates. The one is a technique exploiting $\nu$MOS at blocks in Fig.4, and the other is $\nu$MOS with feedback to synthesis TH gate. Both techniques reduce the number of MOS transistors then higher speed operation is expected.

### B. $\nu$MOS TH gate

The proposed TH gate (hysterisial threshold gate) with feedbacked $\nu$MOS is shown in Fig.10. In case of THmn, the number of feedback inputs $\mid I_f \mid$ is

$$\mid I_f \mid = (m-1). \tag{3}$$

And the number of unit capacitance $\mid C_u \mid$ is

$$\mid C_u \mid = n + (m-1). \tag{4}$$

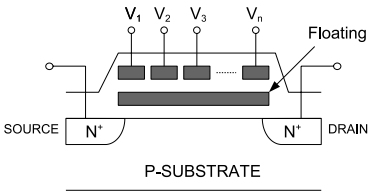


Fig. 6. Structure of $\nu$MOS

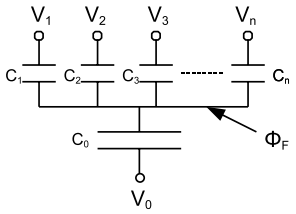


Fig. 7. Eqivalent circuit

Thus initially an $n+m-1$ inputs $\nu$MOS has to be prepared to fabricate THmn.

Instead of the above, a feedback with capacitance;

$$C_f = (m-1) \cdot C_u \tag{5}$$

in a $\nu$MOS can fabricate the same THmn gate.

Let's consider the case $\mid C_u \mid = n+(m-1)$ for simplicity. In Fig.10, when activated inputs are $m$ or more, the output $V_{out}$ goes up HIGH (ON), and the feedback input also activated to ON. In the sequel, $V_F$ goes up by bias voltage $(m-1) \cdot C_u$. Then until all the activated inputs goes down to LOW, $V_{out}$ retains ON because the $V_F$ stays $m \cdot C_u$ or more.

Fig.11 indicates TH23 with $\nu$MOS. The TH23 SPICE simulation results as Fig.12. The result shows when two or more inputs are activated to HIGH, the output goes to HIGH and a feedback input is also activated. Then floating gate voltage $V_F$ is biased by $C_u$ and the output remains HIGH until all input goes down to LOW.

### *C. Block type TH gate with $\nu$MOS*

The second technique is block type TH gate with $\nu$MOS. Block type TH gate has four MOS network blocks. Each block can be defined simple threshold function. Define threshold function $Th(x)$ as;

$$Th(x) = \begin{cases} ON & m' \geq x \\ OFF & otherwise \end{cases} \tag{6}$$

where $m'$ is the number of activated inputs. Then the four blocks in Fig.4 can be synthesized with Th(x). The activating conditions of each block is stated as follows;

GOTO NULL : Th(m)
GOTO DATA : Th(m)
HOLD NULL : Th(1)
HOLD DATA : Th(1)

Therefore, each block can be synthesized only one $\nu$MOS.

Fig.14 is the block type TH23 with four $\nu$MOS's. Clearly Fig.14 is simpler construction than traditional block type th23 in Fig.5. Especially, delay of block type TH gate is depend on GOTO NULL block, then the delay is reduced because GOTO NULL block in Fig.13 has only one transistor. Note that connecting PMOS transistors makes longer delay.

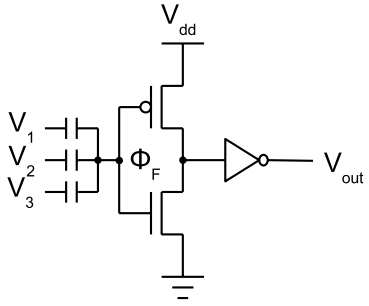


Fig. 8. Three inputs threshold $\nu$MOS gate

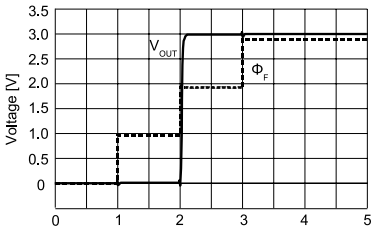


Fig. 9. Characteristic wave form of $\nu$MOS

## IV. Design and Evaluation

We designed THmn gates made from $\nu$MOS with feedback and from block type $\nu$MOS. Some comparison with the number of MOS transistor and delay are provided here. We prepared MOS FET SPICE model provided by MOSIS [12] for simulations. The process rule is TSMC 0.35[$\mu$ m] and supplying voltage is 3.3[V].

And We tried to design THmn gates in a layout level. Fig.15 is TH33 with $\nu$MOS block-type in a layout level. We used MAGIC layout tool [13] in order to design it and chose Poly1-Poly2 technology. Fig.16 is structure of floating-gate using Poly1-Poly2 technology.

On the basis of these, the value of each parameter in TH33 is Table.II.

Table.III shows the comparison of the number of MOS FETs. Clearly, in Table.III, the number of MOS transistors of the proposed circuits is constant irrespectively of the number

TABLE II
PARAMETERS OF TH33

| parameters | value |
|---|---|
| process rule | 0.35 [$\mu$m] |
| $V_{DD}$ | 3.3 [v] |
| $C_1, C_2, C_3$ | 36.0 [fF] |
| $C_0$ | 14.1 [fF] |
| W/L of pMOS | 10.75 [$\mu$m] / 0.75 [$\mu$m] |
| W/L of nMOS | 5.00 [$\mu$m] / 0.75 [$\mu$m] |

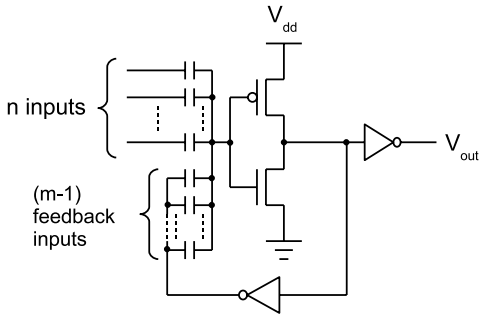


Fig. 10. $\nu$MOS THmn gate

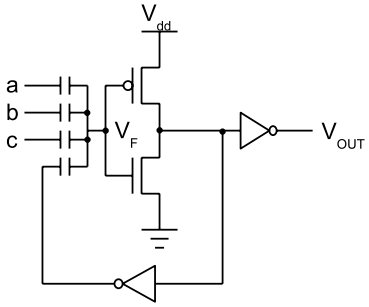


Fig. 11. $\nu$MOS TH23

of inputs or the value of threshold. On the other hand, traditional circuits increase the number of transistors accordance with $n$ and $m$. Therefore proposed circuit technique is adequate for asynchronous systems.

Table.IV shows that the proposed circuits yields fewer delay than traditional circuits. The delay of traditional circuits depends on number of PMOS in GOTO NULL block. Although $\nu$MOS block type is similar structure to the traditional one, it has only one PMOS in GOTO NULL block. Hence the delay of THmn with blocked $\nu$MOS does not depend on the number of inputs or the value of threshold as shown in table.IV.

Finally, a design of asynchronous full adder consists of THmn gate is shown in Fig.17. Note that the symbols, shaped a ginkgo leaf, indicates a THmn gate where a numeral on a symbol is a threshold value of the gate. The computational wave form is also shown in Fig.**??**. This simulation provides favorable operations.

TABLE III
THE NUMBER OF MOS TRANSISTORS

| | Ordinary | THmn with C-$\nu$MOS | Blocked THmn with $\nu$MOS |
|---|---|---|---|
| TH22 | 12 | 6 | 8 |
| TH23 | 18 | 6 | 8 |
| TH24 | 18 | 6 | 8 |
| TH33 | 16 | 6 | 8 |
| TH44 | 20 | 6 | 8 |
| Full Adder | 80 | 24 | 31 |

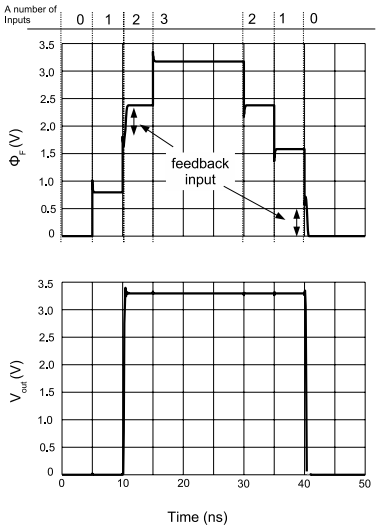


Fig. 12. wave of $V_F$-$V_{OUT}$

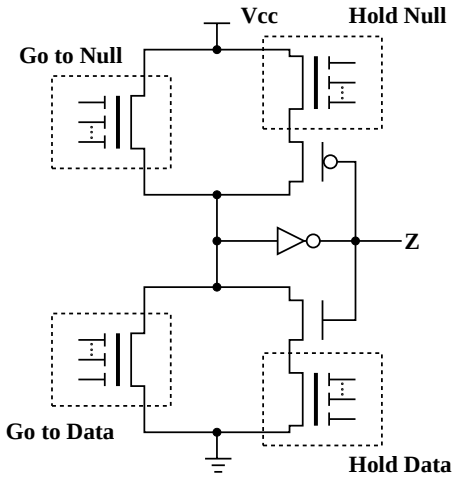


Fig. 13. Block type TH gate with $\nu$MOS

## V. CONCLUSION

In this paper, we proposed exploiting $\nu$MOS to hysterisial threshold gates, which is one of the floating gate, for asynchronous systems. Two types $\nu$MOS TH gates are provided and they are compared with traditional constructed NCL TH gates. As a result, we showed $\nu$MOS TH gates are smaller and faster than traditional one. And the number of MOS FETs and average delay time are efficiently reduced to 62% and 49% compared with traditional one, respectively. As a future work, we will try to design larger circuits like a multiplier.

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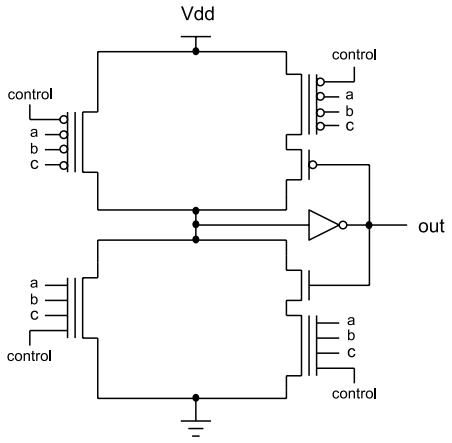


Fig. 14. Block type TH23 with $\nu$MOS

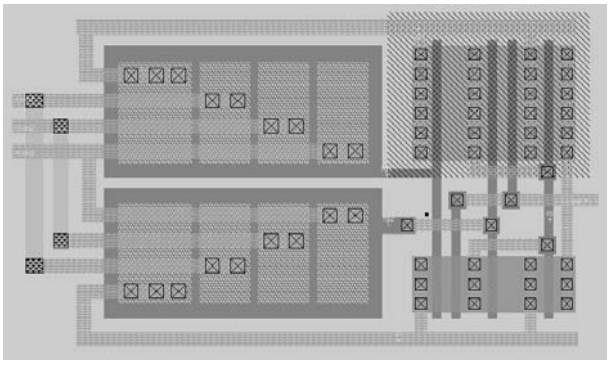

Fig. 15. TH33 layout pattern

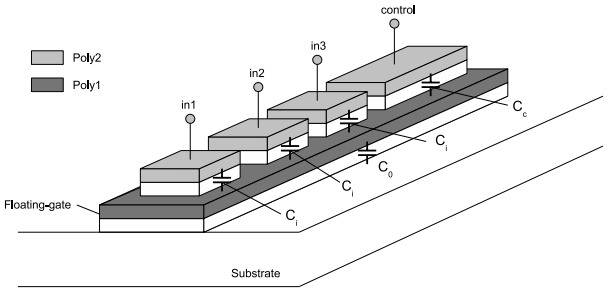


Fig. 16. Structure of Floating-Gate

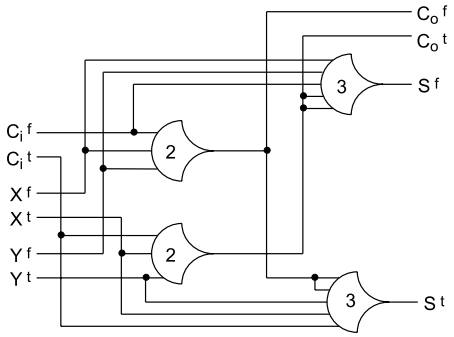


Fig. 17. Full Adder based on $\nu$MOS THmn Gates

turing Gate-Level Weighted Sum and ThreShold Operations", *IEEE Transactions on Electron Devices, Vol.39, No.6(1992)* 1444-1455
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TABLE IV
AVARAGE DELAY OF THGATE [PSEC]

| | Oridinary | THmn with C-$\nu$MOS | Blocked THmn with $\nu$MOS |
|---|---|---|---|
| TH22 | 280 | 160 | 266 |
| TH23 | 450 | 260 | 271 |
| TH24 | 890 | 416 | 390 |
| TH33 | 400 | 197 | 348 |
| TH44 | 535 | 220 | 423 |
| Full Adder | 1041 | 499 | 646 |

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